NNCI ETCH WORKSHOP – SI DRIE IN PLASMATHERM DEEP SILICON ETCHER

Usha Raghuram

Stanford Nanofabrication Facility

Stanford, CA

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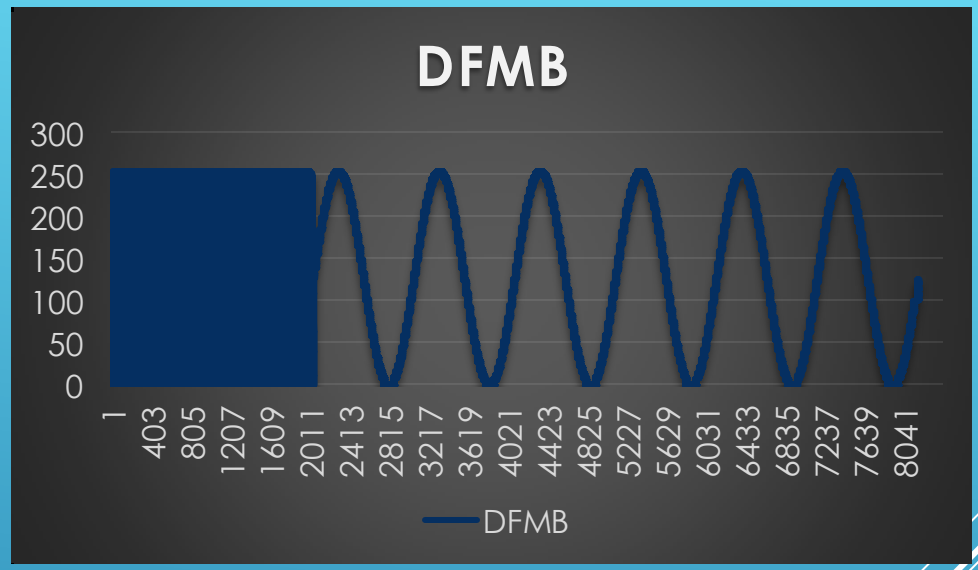
PLASMATHERM DEEP SI ETCHER – PROCESS PARAMETERS

- **Process Parameters/ Limits**
  - Process pressure, Max = 100mT
  - Backside He cooling pressure, max = 10 Torr
  - ICP power 2MHz, max = 3500 W
  - Bias voltage 1kHz-100kHz, max = 1500 V
  - Electrode temp, max = 40 C; min = -40 C
  - Lid temp, Max = 180 C
  - Liner temp, max = 180 C
  - Spool temp, max = 180 C
- **Process gases, max flow**
  - C4F8 = 420 sccm
  - SF6 = 653.4 sccm
  - Ar = 48.5 sccm
  - O2 = 48.25 sccm

PLASMATHERM DEEP SI ETCHER



- Unique Features of PlasmaTherm Deep Si Etcher
  - ICP Power at 2MHz
    - Has a matching network as well as frequency tuning option.
    - Range for frequency tuning – 1.85-2.15MHz
    - Normal mode of operation – frequency tuning for faster tuning
  - ALD valves for the two main gases, C4F8 and SF6 –
    - Gases are always flowing – valve directs the gas to the chamber or to the pump
    - During etch SF6 to the chamber and C4F8 to the pump and during dep vice versa.
    - Enables faster switching between etch and dep
  - Pressure can be controlled by either valve position or pressure set point
  - Bias voltage generator at 100kHz
    - Bias waveform controls switching of bias voltage between 100kHz and 1kHz for SOI process (8msec periods)
  - Morphing function –
    - Selected parameters can be changed as the etch progresses

PLASMATHERM DEEP SI ETCHER – PROBLEMS & FIXES

- Pressure stability – During problem period operated in position control mode
  - Root cause: Throttle valve leak; Fix: Replaced and retrained
- Bias voltage cannot reach set point during the strike step
  - Reset bias generator.
- Black residues on wafer; slow etch rate
  - Chamber clean and conditioning
- DSEC device net nodes off line – Frame IO error
  - DSEC IO connector was loose. Secured the connection

PLASMATHERM DEEP SI ETCHER – PROBLEMS & FIXES

- ICP Reflected power/ impedance errors
  - Occurs periodically mostly from Etch B to Dep step transition and when pressure change is high
  - Thorough chamber clean and conditioning reduces the frequency of errors
  - Run long etches in process in PM, No transfer mode.
  - Installed DSEC computer collect more detailed error log for PlasmaTherm
- Wafer dropped in chamber –
  - Root cause: Resist in clamp area or on the back of the wafer
  - Implemented edge bead removal including wafer flat area;
  - Upgraded the software to include a step for slower lifting of clamp after process.
  - Clamp goes up by a few mm and stops for 30-60 sec (can be programmed) thereby allowing time for wafers to drop off gently back on to the chuck.
  - Need addition steps in recipe.

DEEP SI ETCH – STD RECIPE – QUAL SUMMARY

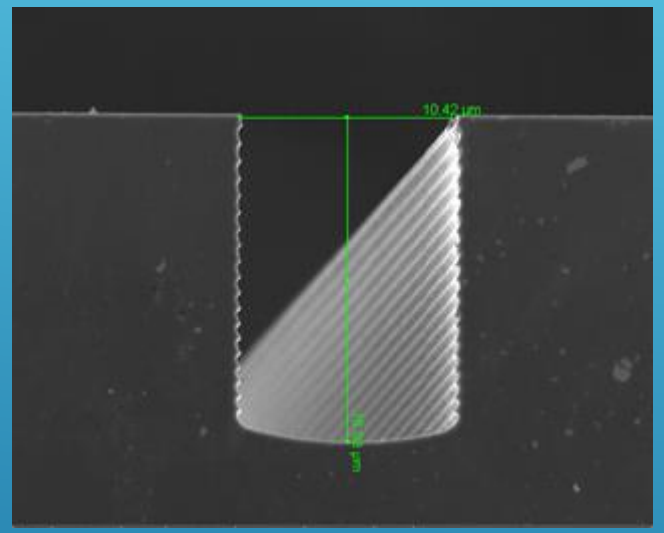
- 4” Si wafers with resolution mask pattern on 1um 3612 photo resist were used
- Pattern density on the wafer is ~25%
- Wafers were etched using the recipe DSE FAT for 20 cycles
- Time in dep step was 2.5s/cycle in recipe 1 and 2.0s in recipe 2
- Otherwise, recipe conditions were identical
- Si step height was measured using Alpha Step and PR on wide features
- The etch rate and selectivity data are as follows:
- Recipe 1: Si Loss/ cycle = 0.9375um; Si ER = 8.035um/min; Si:PR Sel = 107.6
- Recipe 2: Si Loss/cycle = 0.901um; Si ER = 8.317um/min; Si:PR Sel = 100.3
- SEM X-sections were performed through a series of long lines 10-100um wide
- X-Section data indicate no significant difference in Si loss between recipes
- There is an CD dependence for ER up to ~40um for both recipes
- With recipe 2, there is a slight reentrancy in profile on wide features

Depth measurement from SEM X-Section

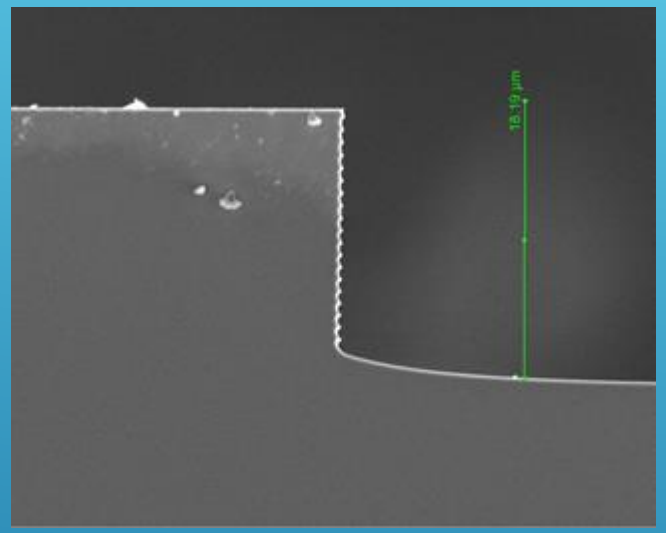
Line Width	Etch depth, um	
	Recipe 1, 2.5s Dep	Recipe 2, 2.0s Dep
10um	16.03	16.07
20um	17.49	17.02
30um	17.98	17.84
40um	18.19	18.2
50um	18.2	18.25
80um	-	18.25
100um	18.2	18.23

Recipe Conditions: BSHe = 4T; Electrode = 15C, Liner = 70C, Lid = 150C, Spool = 180C; No of Cycles = 20
Dep: 150 C4F8, 30 Ar, 25mT, 2000W ICP, 10V Bias, 2-2.5s
Etch A: 150 SF6, 30 Ar, 40mT, 2000W ICP, 250V Bias, 1.5s
Etch B: 300 SF6, 30 Ar, 75mT, 3000W ICP, 10V Bias, 3s

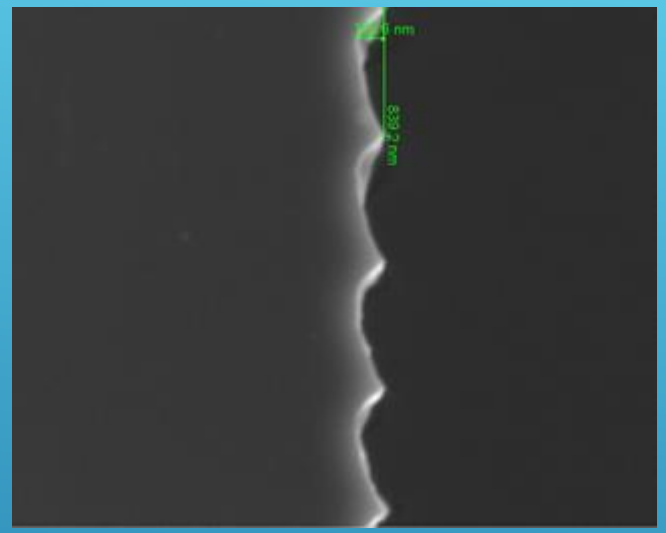
DEEP SI ETCH – STD RECIPE– 2.5S DEP, 1.5S ETCH A, 3.0S ETCH B



- PT-DSE Qual – 10um Line;
- Wafer center
- Sample rotated slightly to see the sidewall striations

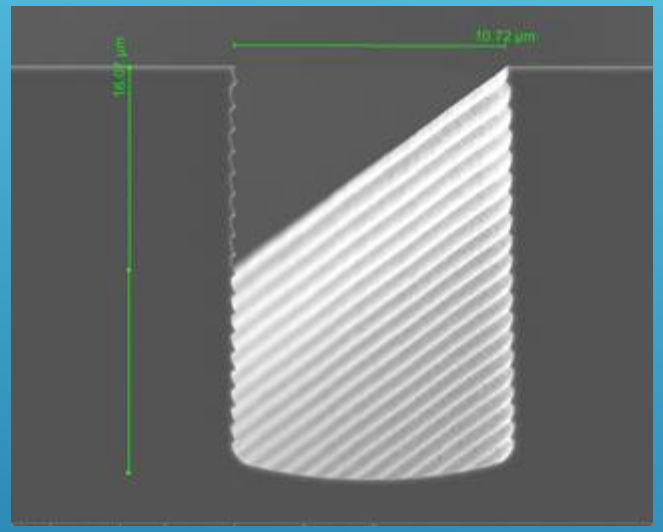


- PT- DSE Qual – Wide Opening
- Wafer Center

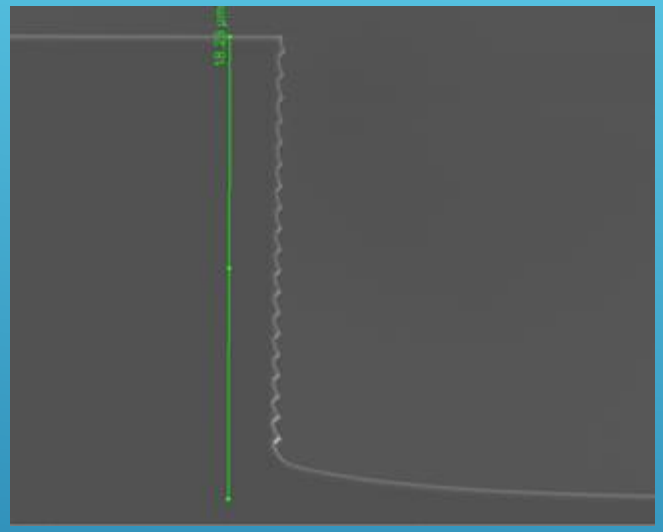


- PT-DSE Qual – Wafer Center
- Scallops in 10um Line – 5th Cycle
- Scallop depth ~166nm

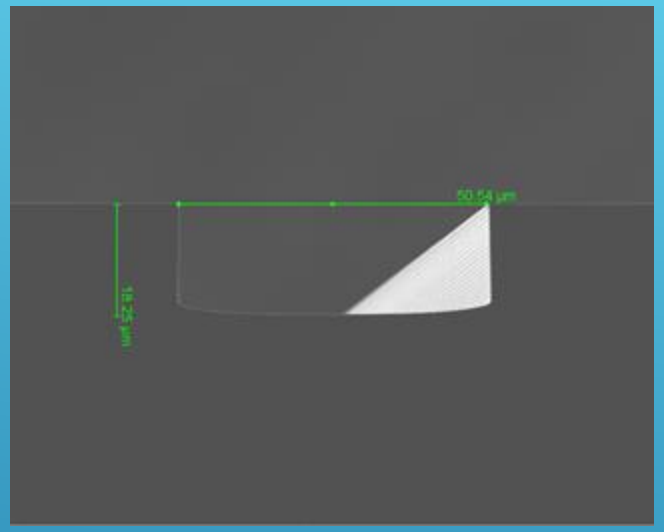
DEEP SI ETCH – STD RECIPE - 2.0S DEP, 1.5S ETCH A, 3.0S ETCH B



- PT-DSE Qual – 10um Line;
- Wafer center
- Sample rotated slightly to see the sidewall striations



- PT- DSE Qual – Wide Opening
- Wafer Center



- PT-DSE Qual – Wafer Center
- Some reentrancy on wider features

DEEP SI ETCH – NANO RECIPE– QUAL SUMMARY

- 4” Si wafers with resolution mask pattern on 1um 3612 photo resist were used
- Pattern density on the wafer is ~25%
- Etch recipe – Nano; Etch rate for wide features (~4um/min; 10um in 50 cycles)

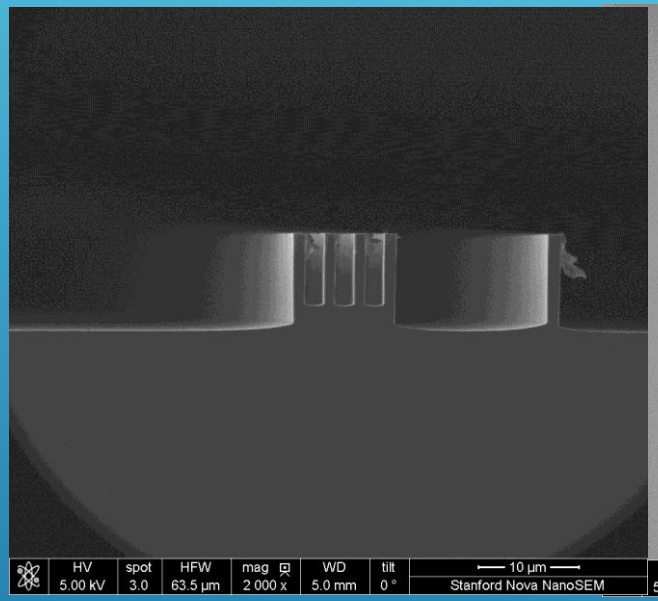
- Recipe Conditions –
- BSHe = 4T; Electrode = 15C, Liner = 70C, Lid = 150C, Spool = 180C; No. of loops = 50
- Dep: 150 C4F8, 30 Ar, 30mT, 1500W ICP, -10V Bias, 1.0s
- Etch A: 150 SF6, 30 Ar, 35mT, 1500W ICP, -350V Bias, 1.0s
- Etch B: 50 SF6, 30 Ar, 25mT, 1300W ICP, -10V Bias, 1.0s

- SEM X-sections were performed through a series of long lines 10-100um wide as well as 1.5-5um wide lines
- There is an CD dependence in loss up to ~20um and there is a slight reentrancy in profile; Pre-etch x-section for incoming resist profile is not available.

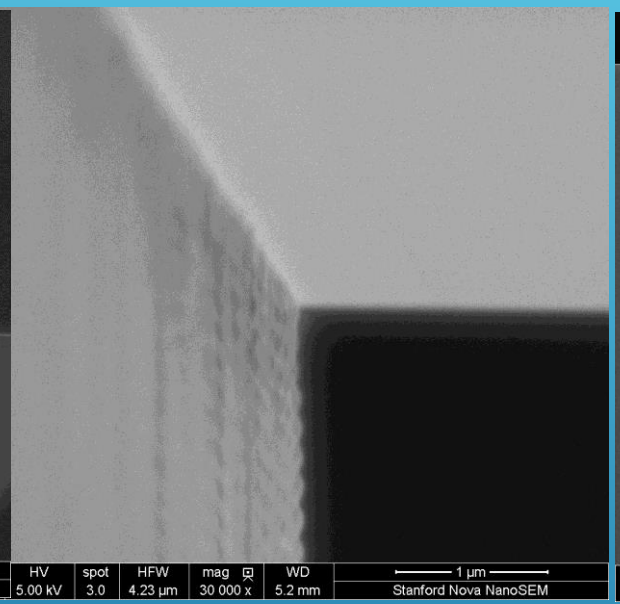
Depth measurement from SEM X-Section

Trench Dimension, um	Etch Depth, um
1.5	7.193
2.0	7.442
2.5	7.705
3.0	7.984
3.5	8.201
4.0	8.356
4.5	8.558
5.0	8.646
10	9.709
20	9.953
30	9.922
40	10.05
50	10.01
80	9.953
100	9.984

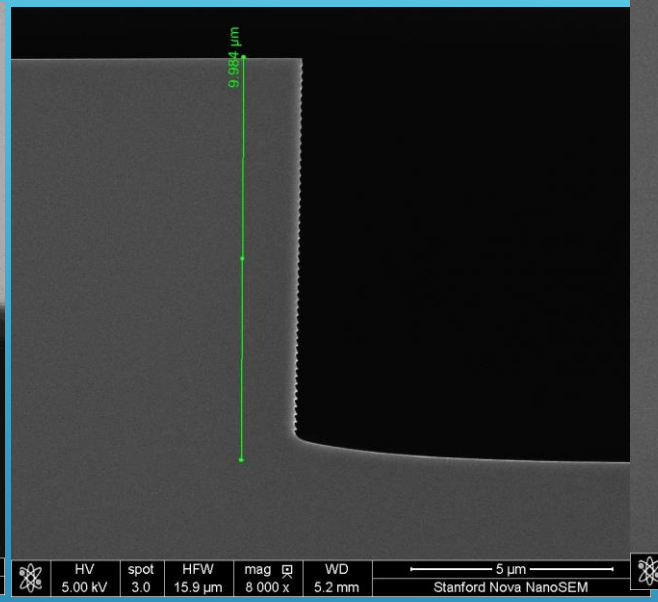
DEEP SI ETCH – NANO RECIPE



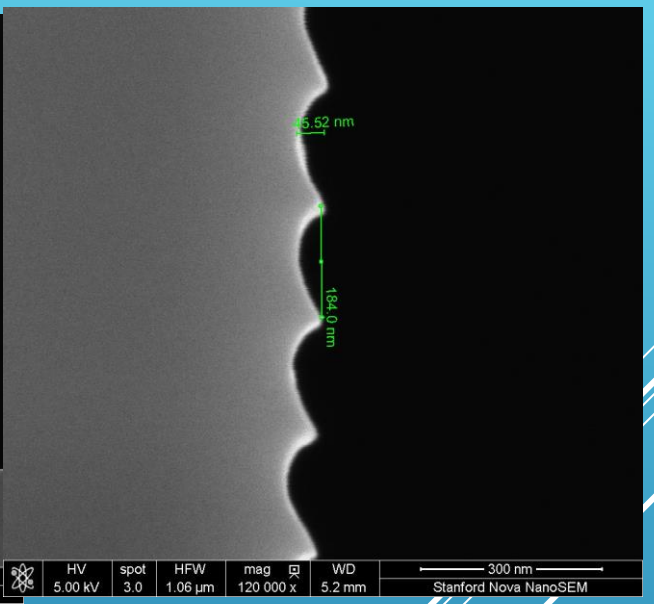
- Etch Depth dependence on trench dimension



- Wide Opening - Wafer Center
- Sidewall View



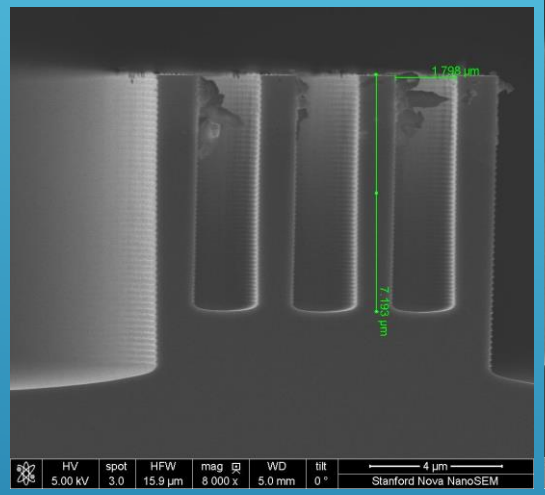
- 100um wide -Wafer center
- Etch depth = 9.984um
- Etch Rate 3.994um/min



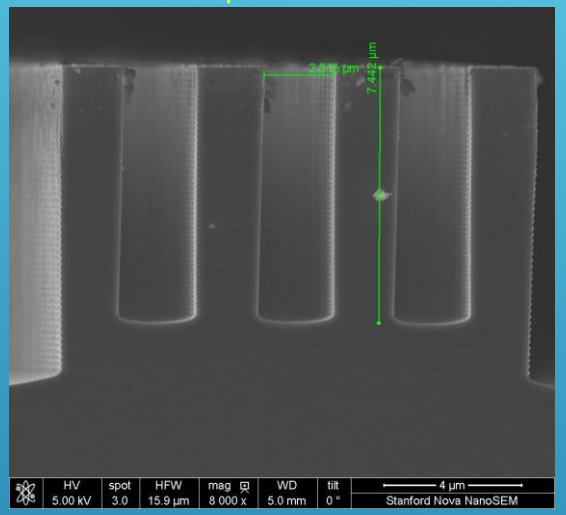
- Scallops in 100um Line
- Scallop depth ~45.5nm

DEEP SI ETCH – NANO RECIPE – TRENCH DEPTH VS CD

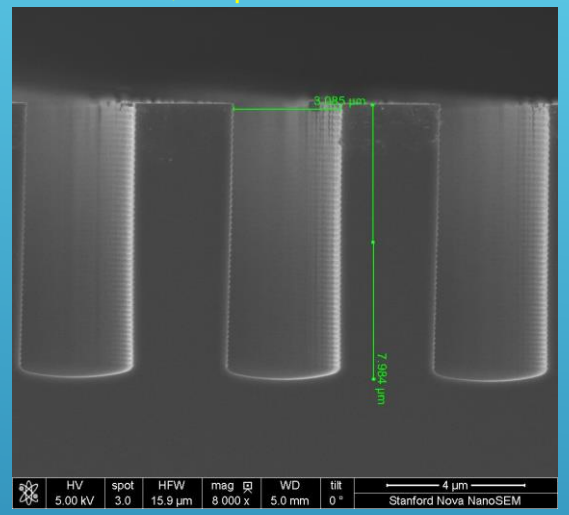
1.5um Line; Depth = 7.193um



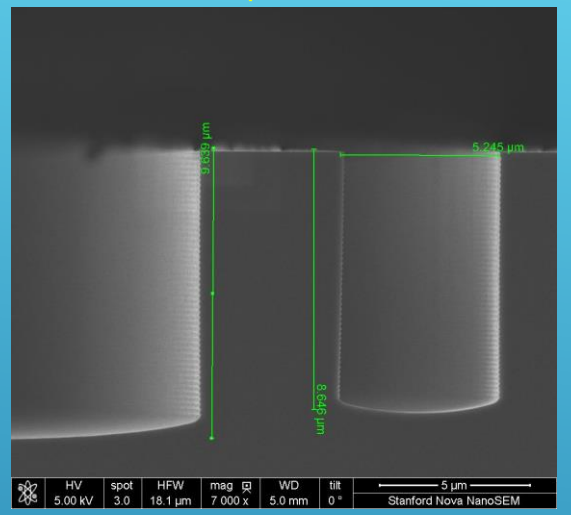
2um Line; Depth = 7.412um



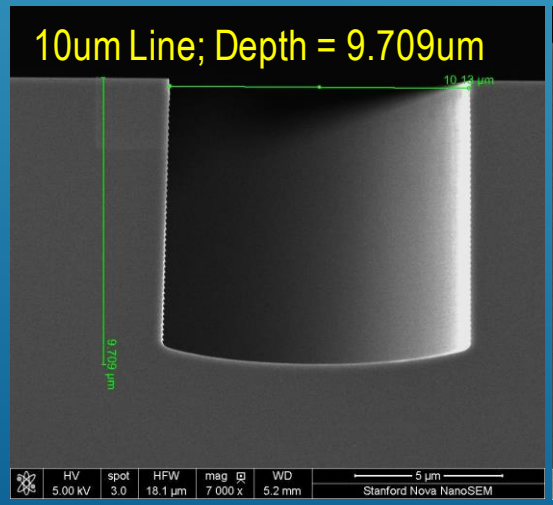
3um Line; Depth = 7.984um



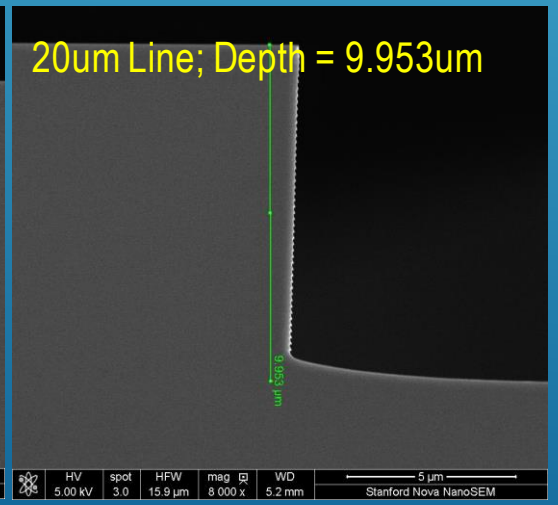
5um Line; Depth = 8.646um



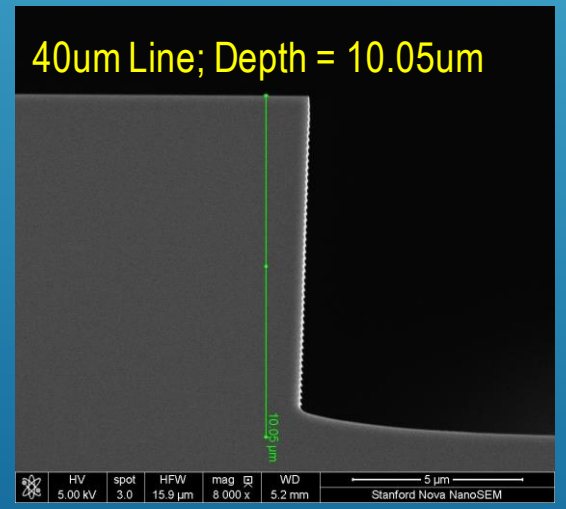
10um Line; Depth = 9.709um



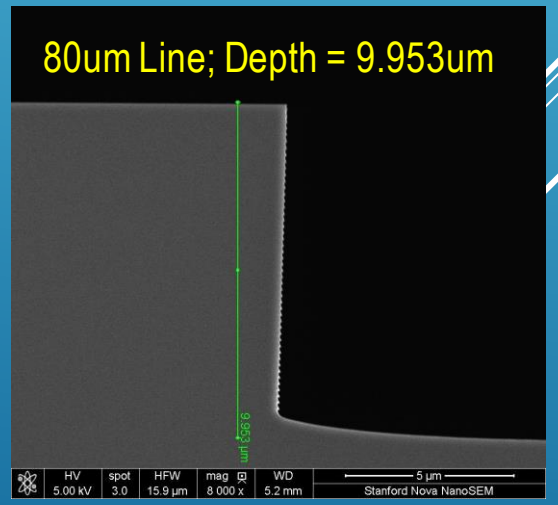
20um Line; Depth = 9.953um



40um Line; Depth = 10.05um



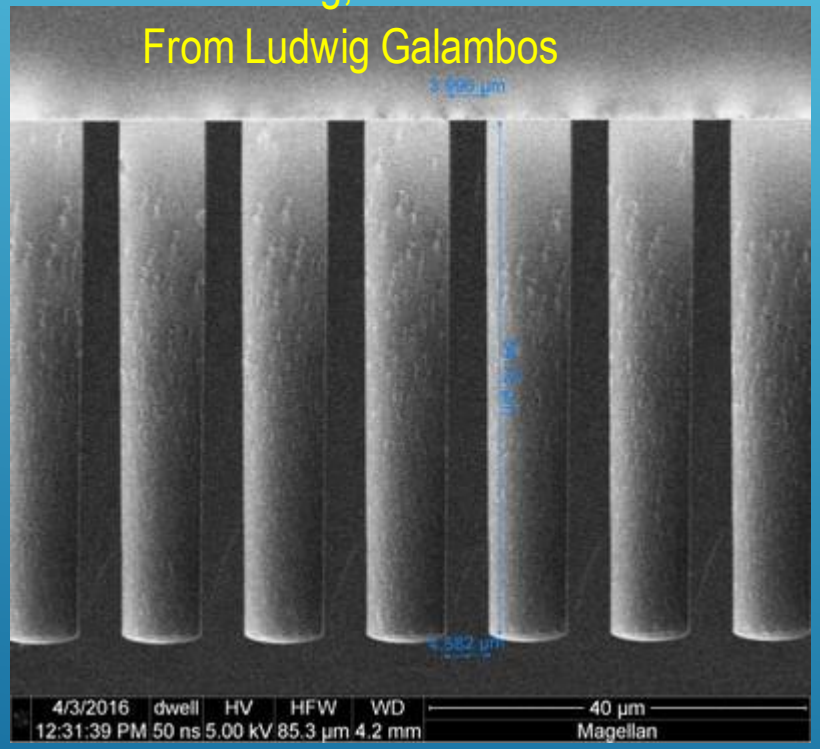
80um Line; Depth = 9.953um



DEEP SI ETCH – NANO RECIPE – 500 CYCLES (55UM DEEP)

4um Grating; 2.19um/min

From Ludwig Galambos



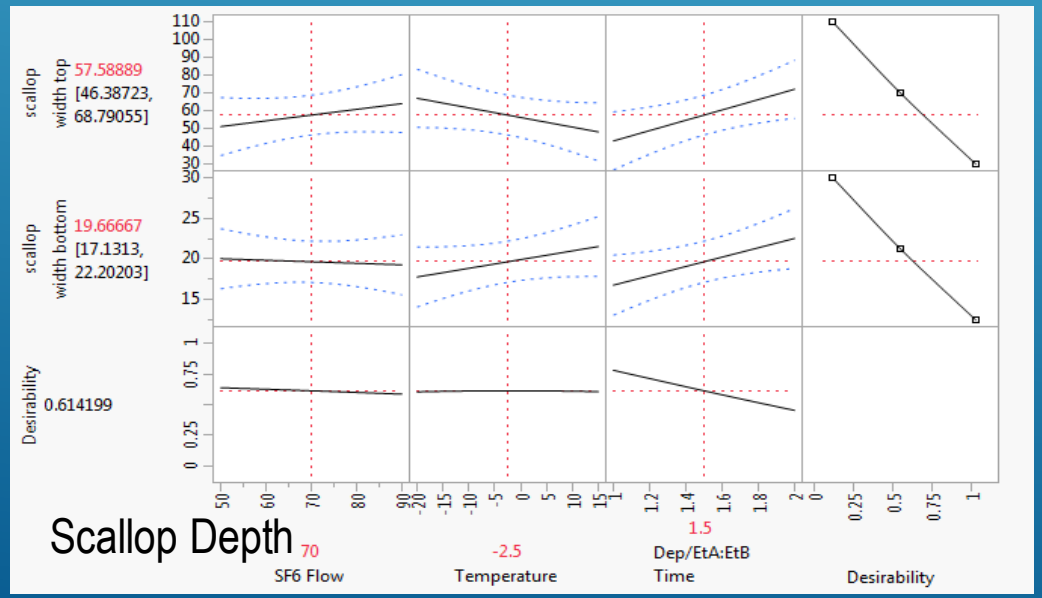
DEEP SI ETCH – SMOOTHER SIDEWALLS – DOE ANALYSIS

- DOE Purpose: To minimize scalloping and undercut
- Mask: Oxide hard mask
- DOE Constants:
- ICP Power = 1500W Dep, Etch A and Etch B; Bias Voltage = 10 W dep, 250W etch A, 10 W, etch B; Pressure = 30 mT dep; 35mT etch A and 40mT etch B; Ar = 30 sccm; C4F8 (dep) = 150sccm; Number of cycles = 100; Temp = Liner = 70C; Lid = 150C; Spool = 180C
- Optimized Process (PT-Smooth) from DOE: SF6 (Etch B) = 100sccm; SF6 (Etch A) = 150sccm; Temperature = -20C; Time = 1s (dep, Etch A and Etch B steps)

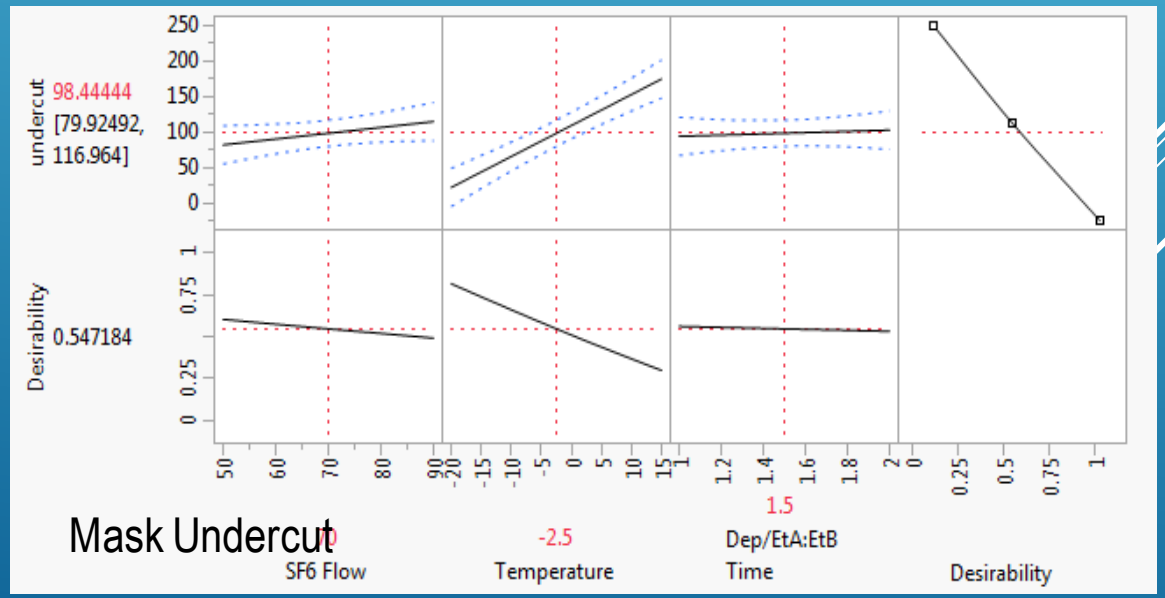
DOE Variables

	Pattern	SF6 Flow	Temperature	Dep/EtA:EtB Time
1	+++	90	15	2
2	000	70	-2.5	1.5
3	+−+	90	-20	2
4	−−−	50	-20	1
5	−−+	50	-20	2
6	−+−	50	15	1
7	+−−	90	-20	1
8	++−	90	15	1
9	−++	50	15	2

Data and analysis are part of Andrew Ceballos & Stephen Hamann's Fall 2014 EE412 project

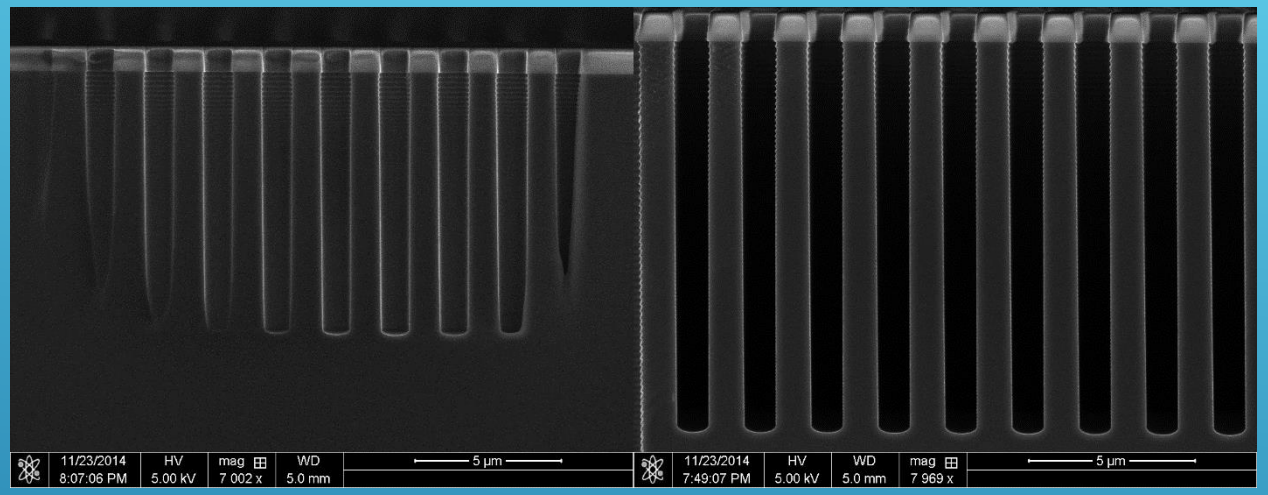


Scallop Depth

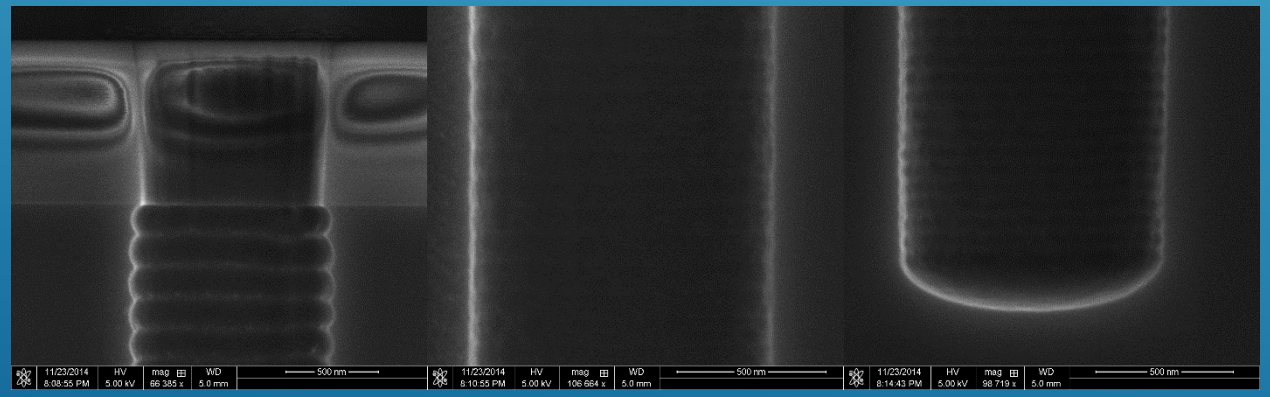


Mask Undercut

DEEP SI ETCH – RECIPE FOR SMOOTHER SIDEWALLS



Etch results for 1um holes left, and 1um lines and spaces.

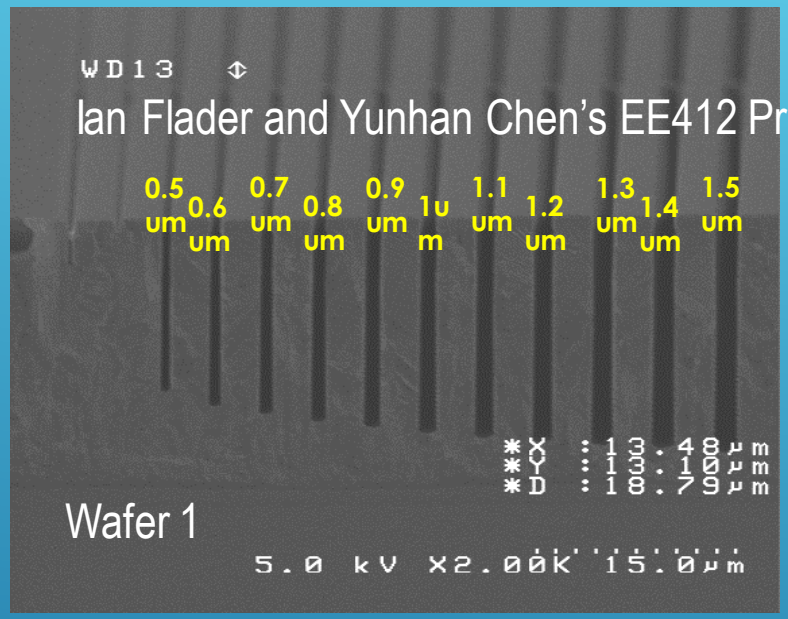


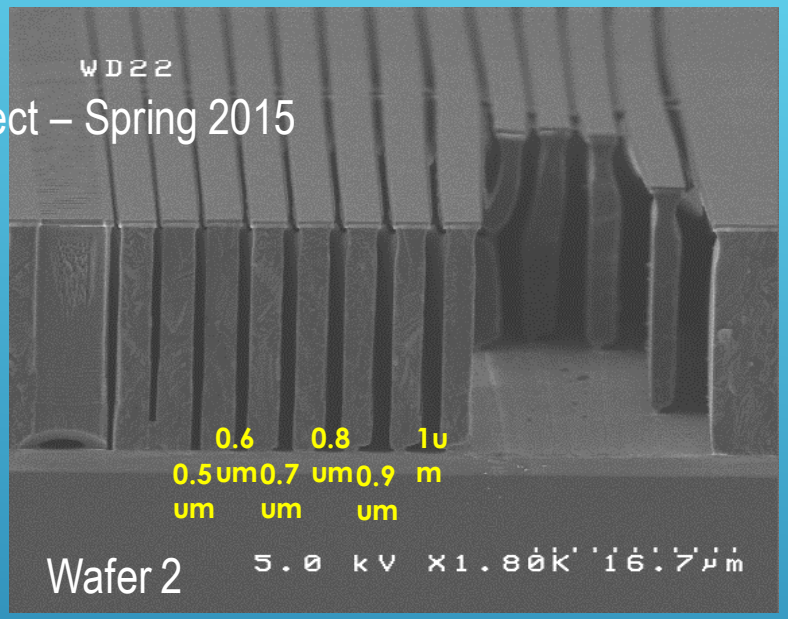
Magnified images of various sections of the etch profile in a 1um hole

Data and analysis are part of Andrew Ceballos & Stephen Hamann's Fall 2014 EE412 project

- 1um lines and 1um holes were chosen for the investigation.
- Scallops were deeper in the top (~40nm) and none in the middle (<5nm) and minimal (~20nm) in the bottom for both holes and lines for the optimized recipe.
- Scallop depth variation was analyzed for both top and bottom sections (DOE analysis and conditions in the next slide.
- Both sections showed that a lower deposition and etch a times resulted in less scalloping with a strong statistical significance (p value = 0.034 top and 0.044 bottom).
- There also appears to be a weak but somewhat significant evidence for dependence on temperature (p value = 0.075 top and 0.095 bottom).
- Electrode temperature does greatly affect the undercut (p value = .0035), with their being practically no undercut at -20 C.
- This result is likely due to improved initial polymer deposition at the lower temperature.

SOI PROCESS – UNDERCUT WITH ORIGINAL RECIPE





- Original recipe was based on PlasmaTherm recommended process
- No of cycles for loop 1 and 2 were chosen such that there is some unetched Si at the end of loop 2 and profile was acceptable (refer to SEM from wafer 1)
- Wafer 2 was etched with the same number of cycles as in the case of wafer 1 plus an additional 90 cycles in loop 3 where the bias waveform was set to 3 (25% on 100kHz bias V)
- As can be seen from SEM, smallest features were not cleared while wider lines were notched.
- There were issues with bias voltage generator and so, wafers were sent to PlasmaTherm for further development.

Loop 1 - No of cycles = 20

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	30
Ar sccm	30	30	30
Pressure	30	35	40
ICP watts	1500	1500	1500
V p-p	10	250	10
waveform	1	1	1
Step time (s)	1.5	1	1

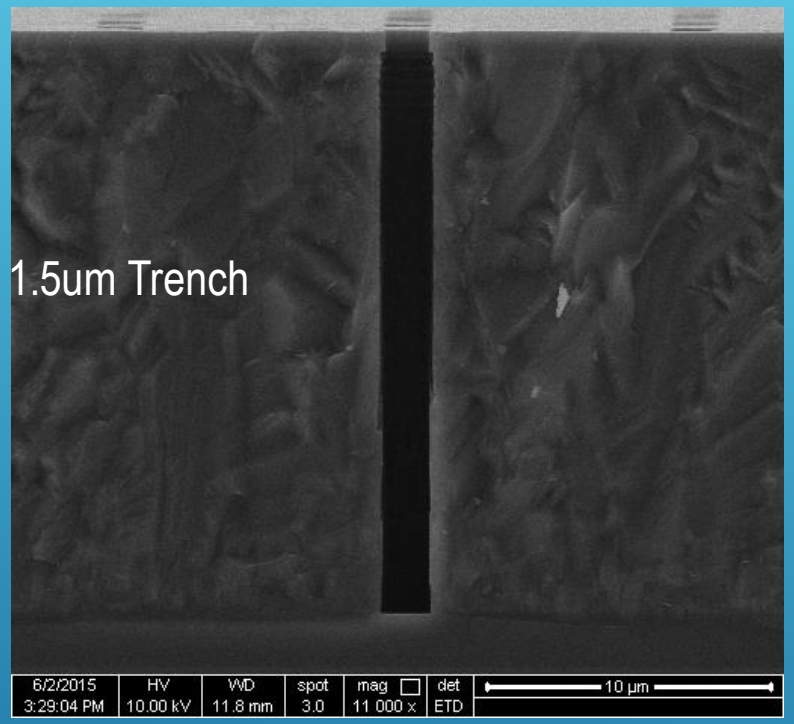
Loop 2 - No of cycles = 34

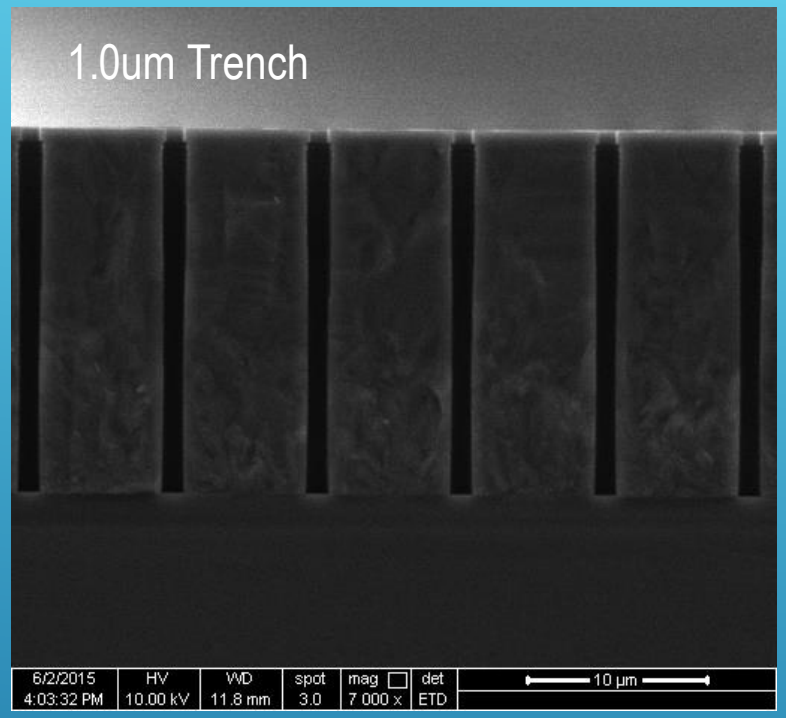
Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	250
Ar sccm	30	30	30
Pressure	25	40	60
ICP watts	2000	2000	2000
V p-p	10	250	100
waveform	1	1	1
Step time (s)	2.3	1	1.5

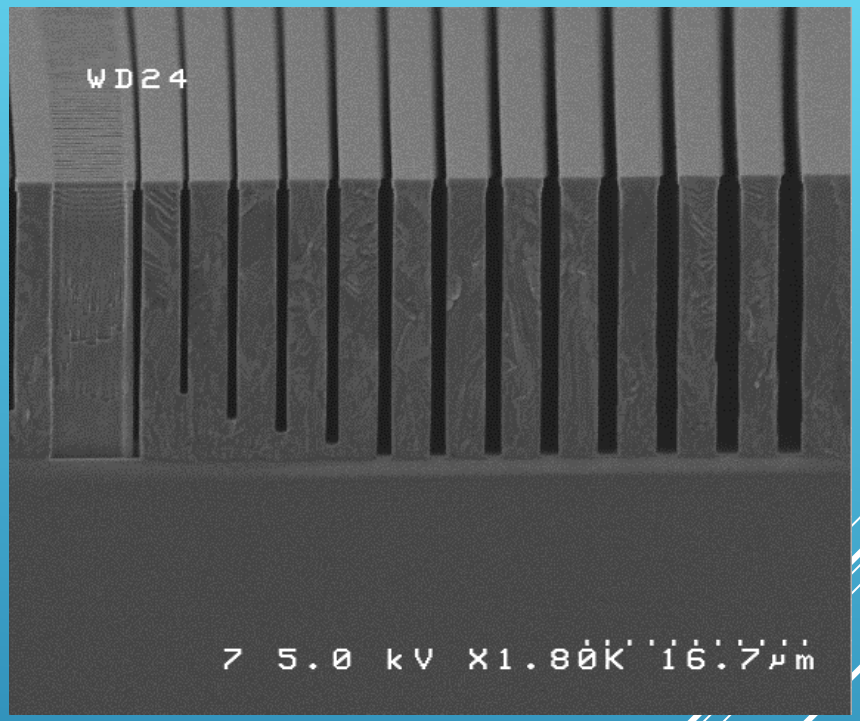
Loop 3 - No of cycles = 90

Parameter	Dep	Etch A	Etch B
C4F8 sccm	125	15	15
SF6 sccm	*75 to pump*	75	100
Ar sccm	30	30	30
Pressure	20	20	20
ICP watts	1600	1250	1250
V p-p	10	400	215
waveform	3	3	3
Step time (s)	2	2	1.5

IMPROVED SOI ETCH FROM PLASMATHERM







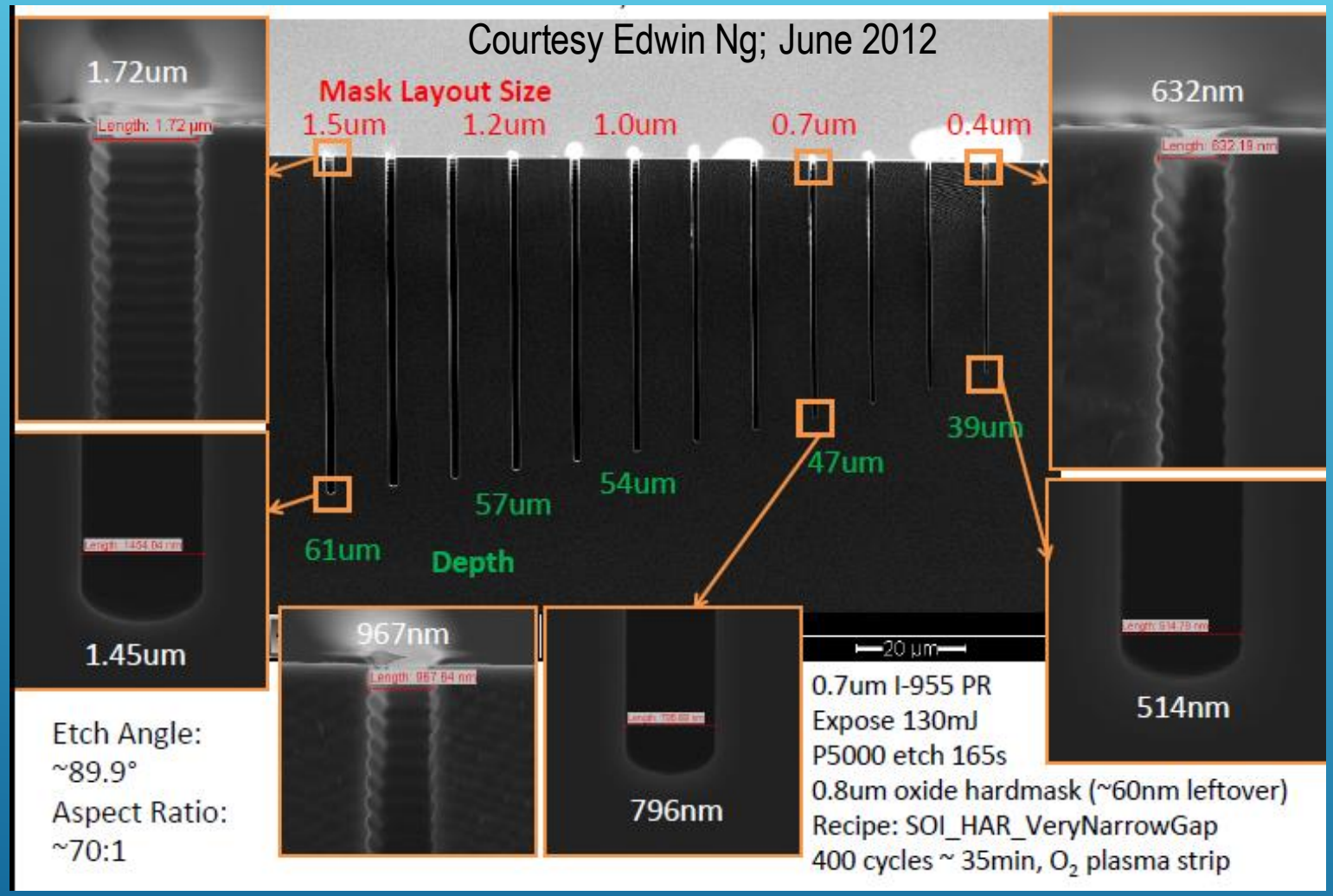
- Recipe much improved and all features down to 1 um have no notching.
- Sub micron features did not get etched down to SiO2.
- There is some minor undercut at the mask

IMPROVED SOI ETCH FROM PLASMATHERM

Parameter	Dep	Etch A	Etch B	Dep2	Etch A2
C_4F_8 (sccm)	150	(150 to pump)	(150 to pump)	125	15
SF_6 (sccm)	(150 to pump)	150	150	(100 to pump)	100
Ar (sccm)	30	30	30	10	10
Pressure(mTorr)	25	40	45	20	30
ICP (W)	2000	2000	1000	1700	1500
Bias (Vp-p)	10	300-350(1)	10	10	600
Waveform	1	1	1	3	3
Step time (sec)	2	1.5	1.5	1	4
Loops	48 loops (4 min)			60 loops (5min)	
Electrode temp	15 C				

Parameter	Result
Etch rate (μm/min)	3.3
Selectivity (Si:PR)	50:1
Profile	90.1°
Undercut (μm)	~0.4
Notching (μm)	~0.1

RESULTS FROM STS HRM ETCHER



- No SOI pictures; but SOI recipe was used.
- Etch rates bit slower than the DSE recipe.
- Both tools are able to etch sub micron features.
- Aspect ratio dependence comparable.
- Similar scallop depths.
- Process trends similar between the tools

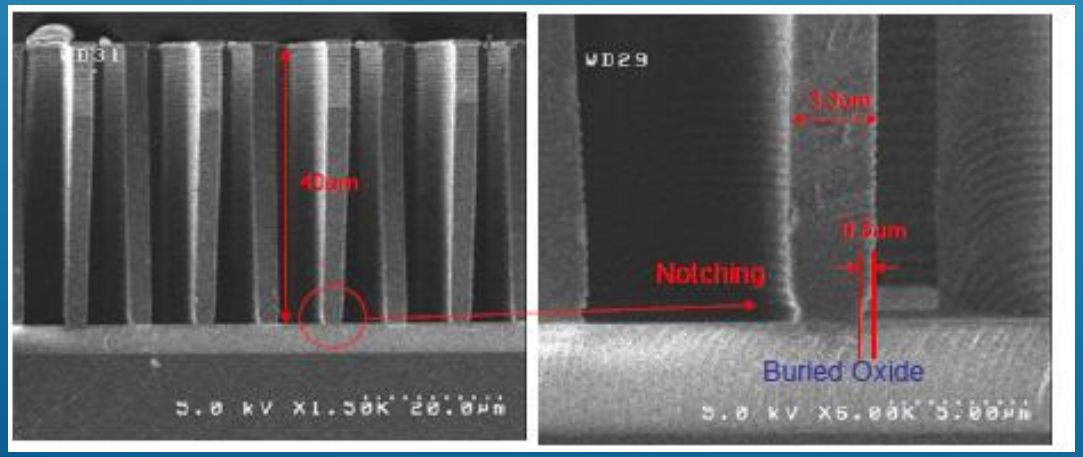
PROCESS TRENDS AND SOI ETCH -STS HRM ETCHER

Courtesy Jae Woong Jeong

Trends for Controlling process results	Etch rate	Profile (↑ negative) (↓ positive)	Selectivity	Grass	Breakdown	Sidewall Roughness
Etch gas increase	↑↑	↑↑	↑	↓	↑	↑
Dep gas increase	↓↔	↔	↑	↑	↓↔	↓
Etch:Dep time ratio increase	↑	↑	↑↔	↓	↑↔	↑
Pressure increase	↑↑	↑	↑	↓↔	↑	↑
Dep Coil Power increase	↓↔	↓↔	↑↔	↑	↓↔	↓
Etch Coil Power increase	↑	↑	↑	↓	↑	↑
Platen Power increase	↑↔	↑↔	↓	↓	↔	↔
EM1 value (e) increase	↓↔	↓↔	↑	↑↔	↓↔	↔
EM1 delay (e) increase	↑↔	↑↔	↓	↓↔	↑↔	↔

E=etch
↔ no effect or negligible effect
↑ increase
↓ decrease

SF6/O2 Flow (sccm)	C4F8 Flow (sccm)	Etch Cycle Time (s)	Dep. Cycle Time (s)	
450/45	100	3	2	
Pressure (pass/etch)	**Coil Power (pass/etch)**	**Platen Power (pass/etch)**	**EM/Delay**	**Temp**
15%/15%	1000W/2400W	0W/45W	0A/0s	10C



- Some notching with SOI recipe as well as undercut with overetch on SOI processes in both equipment.
- Process trends similar between the tools
- Main difference is:
  - In STS HRM, the bias power can be cycled between on and off to dissipate the charge accumulated at the oxide interface
  - In PlasmaTherm DSE ,it cycles between 100 and 1kHz.

SUMMARY

- Results from four different processes on PlasmaThem Deep Si etcher were provided.
- Performance of PlasmaTherm etcher is comparable to sts HRM etcher.
- SOI etching performance is similar between the tools.
- Main difference is that the bias power can be cycled between on and off for SOI overetch in STS HRM while is cycles between 100-1kHz in PlasmaTherm.