



# End-point Detection for Plasma Etching – *Knowing When to Stop*

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Lead Applications Engineer (Deposition)  
NCCI Etch Symposium 2022 @ UPenn

# About The Presenter: Joshua Perlstein



- Currently a lead applications engineer for SPTS North America (deposition products), I went to school at the University of Central Florida where I got degrees in mechanical engineering (BS) and materials science (MS); I worked with optical thin films and device fabrication heavily in graduate school.
- I have worked previously as a process development engineer, manufacturing equipment engineer, and field service engineer.
- I like airplanes, houseplants, the great outdoors, travel, and watching wafers move around a fab.

# About SPTS Technologies

A leading manufacturer of etch and deposition process solutions and equipment for the semiconductor manufacturing industry

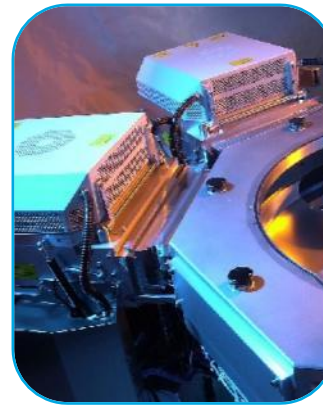
- SPTS Technologies is part of the Electronics, Packaging and Components (EPC) Group of KLA Corp.
- Global presence – operate across 19 countries
  - Headquartered in the UK
  - Manufacturing sites in UK and US
- Support our customers with local Sales and Service teams



Etch



PVD



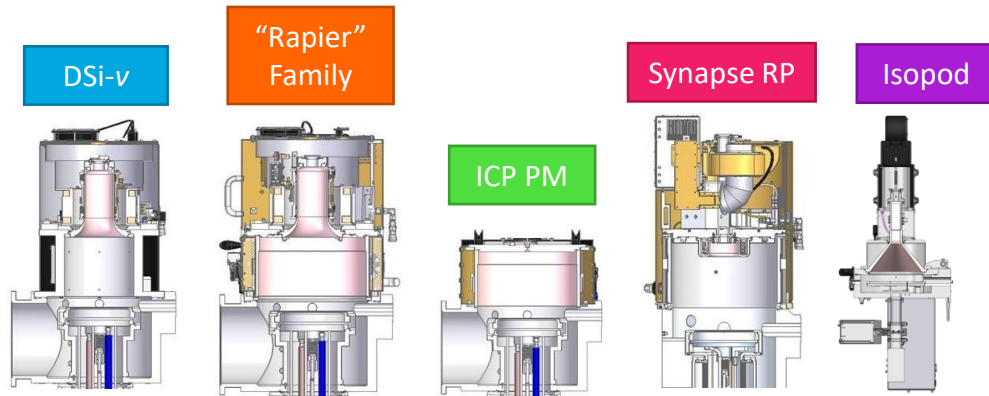
PECVD



Release Etch  
& MVD

# Contents

## SPTS Etch Product Line (5x module types)

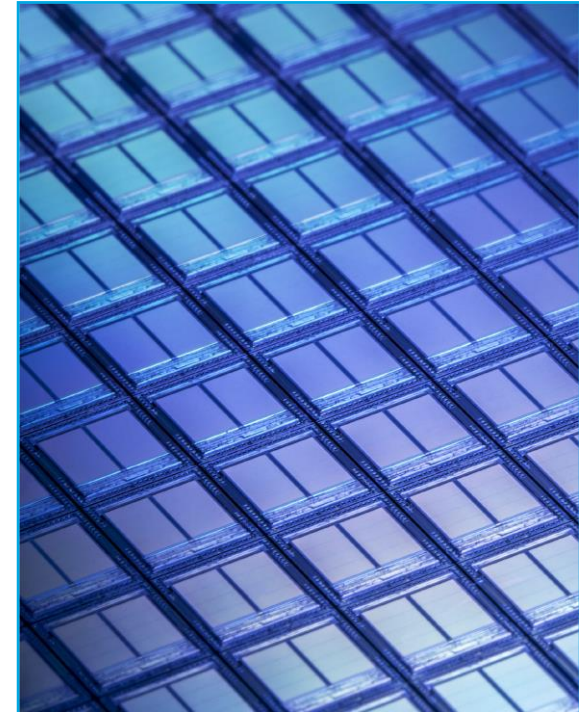


- What is End-point Detection (EPD)?
- Why do we need EPD?
- What methods exist for EPD?
- 'Troublesome' etches?

- Examples of EPD for Critical Etch Applications ....
  - **Parametric**
  - **Optical Emission Spectroscopy (OES)**
    - Including Claritas™
  - **Reflectance & Interferometry**
    - White Light
    - Visible LASER
    - Near infrared LASER
  - **Image Capture** - ReVia®, Ascent™
- Summary table of EPD methods
- Conclusions

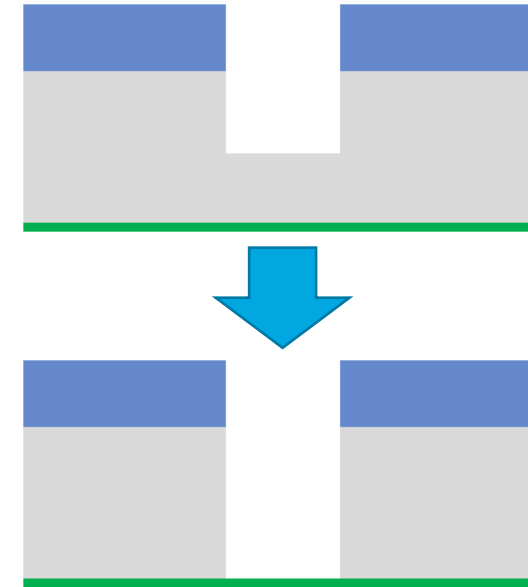
# What is End-point Detection?

- Plasma Etching
  - Critical step in fabrication of all semiconductor devices and most other microfabricated devices.
- Important to know when the process is complete
- Techniques employed to detect the process completion point, or a point in the process prior to completion, are referred to as '*End-point Detection (EPD)*'



# Why Do We Need EPD?

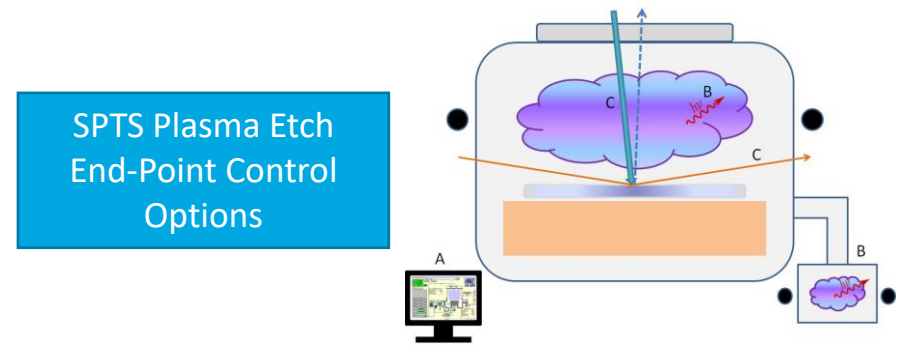
- Time based etching has limitations
  - Variations in film thicknesses
  - Variations in film composition or density
  - Variations in etch rate – from chamber condition
- End-point Detection offers benefits
  - Etch time can ‘float’ – reducing test wafers
  - Track certain layers or depths
  - Modify process eg when we reach a stop layer
  - Improve process repeatability
  - Prevents under-etching → eliminating scrap or re-work
  - Prevents over-etching → **better CD control, better sidewall quality**  
**better under-layer loss, better notching**  
**better throughput, better device performance**  
**better Yield**



EPD selling price can be 8-12% of the Process Module  
But ROI can be very short  
99% of all Etch PMs shipped have an EPD of some sort

# End-point Detection Methods

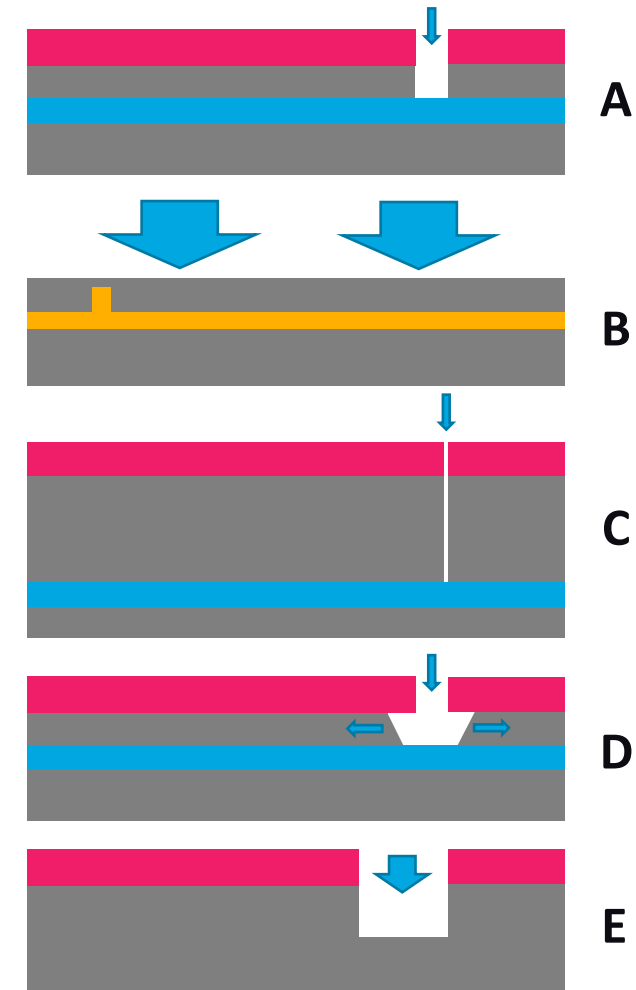
- EPD requires an aspect of the process that changes with time
  - Either as the etch depth increases
  - Or as different layers in the wafer are reached
- Three categories of EPD
  - Etch system monitoring – ‘Parametric’ (A)
  - Plasma or gas monitoring (B)
  - *In-situ* wafer monitoring (C)



	Method	Monitors	Based on
A	Parametric	<b>System</b>	APC angle or He flow
B	Optical emission spectroscopy (OES)	<b>Plasma</b>	Glow from plasma
	Claritas		Re-ignited glow from plasma
C	WL Reflectance	<b>Wafer</b>	Reflection
	WL Interferometry		Broad area interferometry
	LASER interferometry		Small spot interferometry
	NIR		Broad area interferometry
	ReVia, Ascent		Wafer vision

# 'Troublesome' Etches

- **A.** Very low open areas
  - <1%, eg. Back Side Vias (Si, GaAs, SiC)
- **B.** Very high open areas
  - >99%, eg. Via Reveal
- **C.** High aspect ratios
  - eg. SOI at 50:1 AR
- **D.** Etching doesn't stop
  - eg. tapered TSVs
- **E.** Blind etches – with no under-layer
  - eg. Bulk thinning or Power Trenches
- Wafers/chemistry prevent standard methods
  - eg. Ni or Cu masked SiC Via etching (SiF\* optical emission is suppressed by presence of metal mask)

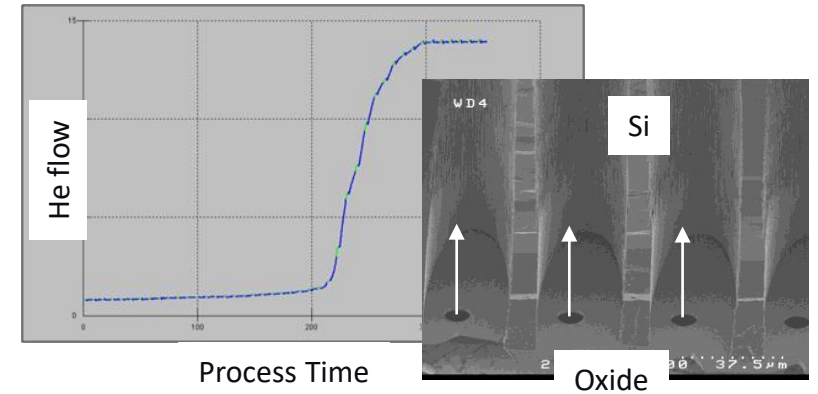




# Parametric EPD

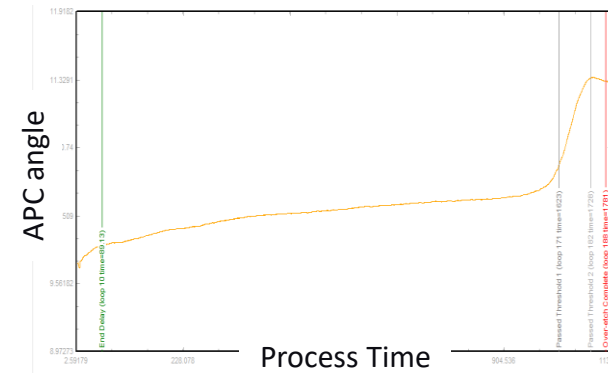
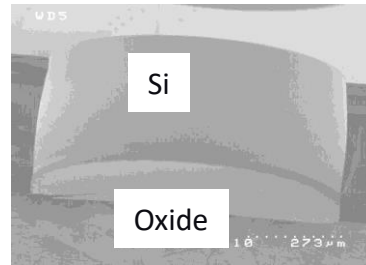
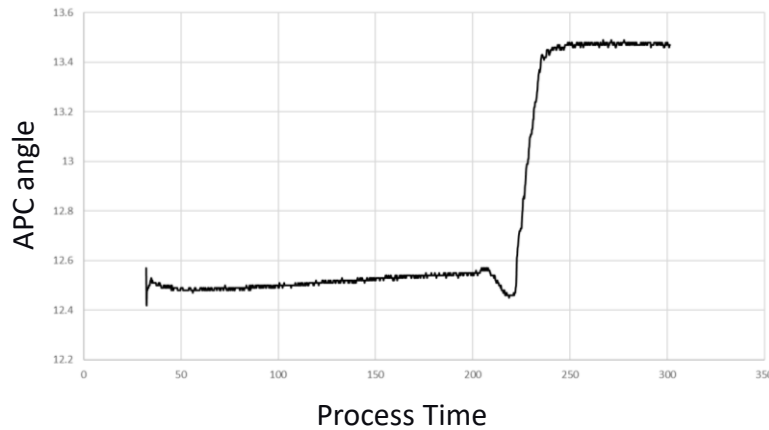
- Based on Etch system datalogs – FOC!
- APC valve position or He back side pressure flow rate

## Si trenches for inkjet nozzles



## Si Cavities for Microphones

### Blanket Si etch-off for FO-WLP



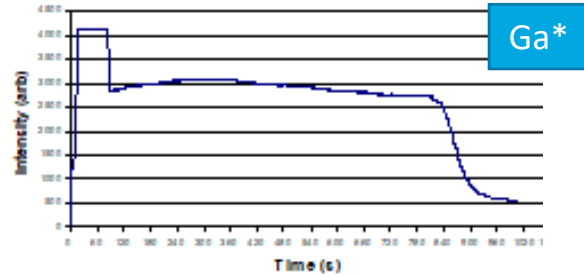
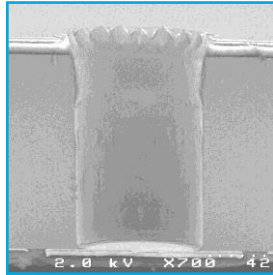
# Plasma or Gas Monitoring

Technique	Cost	Benefits (+)	Disadvantages (-)
<b>LASER Induced Fluorescence (LIF)</b>	\$\$\$\$	<ul style="list-style-type: none"> <li>• Provides some detail of plasma chemistry</li> </ul>	<ul style="list-style-type: none"> <li>• Limited to species that fluoresce</li> <li>• Difficult to interpret data</li> <li>• Affected by plasma glow</li> </ul>
<b>Mass Spectroscopy (e.g. RGA)</b>	\$\$\$	<ul style="list-style-type: none"> <li>• Analyses all species</li> </ul>	<ul style="list-style-type: none"> <li>• Intrusive to plasma</li> <li>• Needs high vacuum (differential pumping)</li> <li>• Species are ionised/cracked before detection</li> <li>• Difficult to interpret data</li> <li>• Low filament lifetime in chemical plasmas</li> </ul>
<b>Optical Emission Spectroscopy (OES)</b>	\$\$	<ul style="list-style-type: none"> <li>• Widely applicable</li> <li>• Easy to use &amp; interpret</li> </ul>	<ul style="list-style-type: none"> <li>• Limited to species that are emitting light</li> </ul>
<b>Langmuir Probe</b>	\$	<ul style="list-style-type: none"> <li>• Easy to use</li> </ul>	<ul style="list-style-type: none"> <li>• Intrusive to plasma</li> <li>• Limited to ion &amp; electron information</li> <li>• No chemistry information</li> <li>• Difficult to interpret</li> </ul>

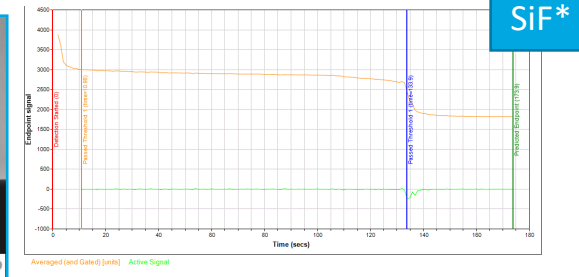
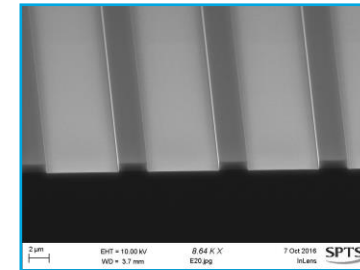
- OES is preferred method for Plasma Monitoring

# Optical Emission Spectroscopy (OES)

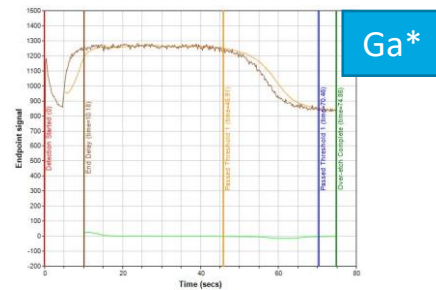
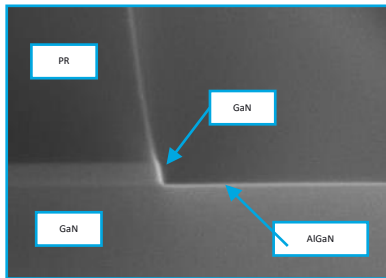
GaAs back side Via  
RF device



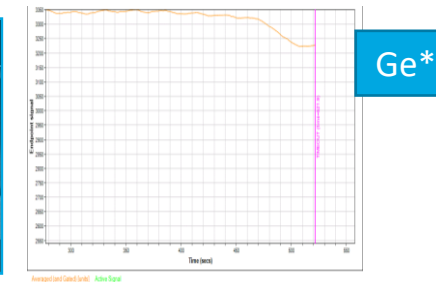
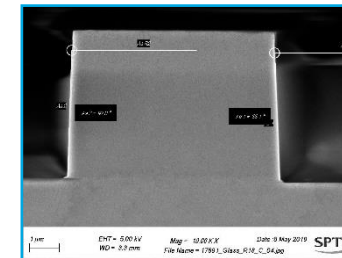
Oxide mask open  
MEMS device



GaN to AlGaN etch  
Power device

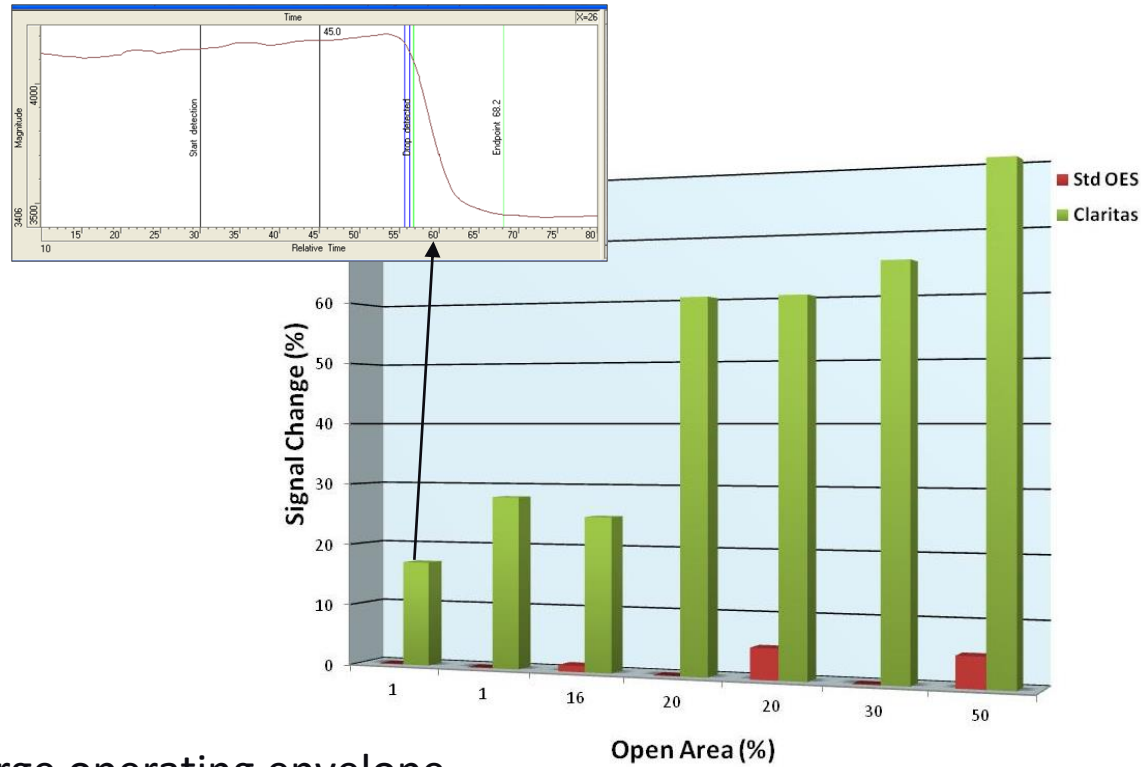


Ge-doped core etch  
Photonics device

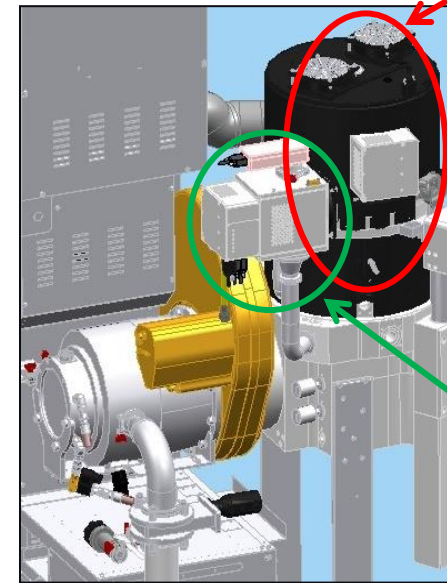
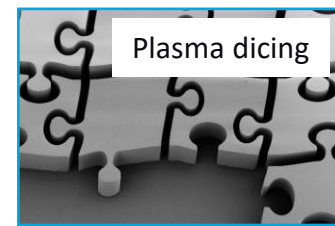
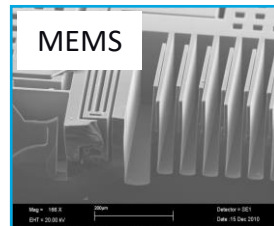


- Also used for inter-wafer cleans of the process module

# Claritas™ (Patented)

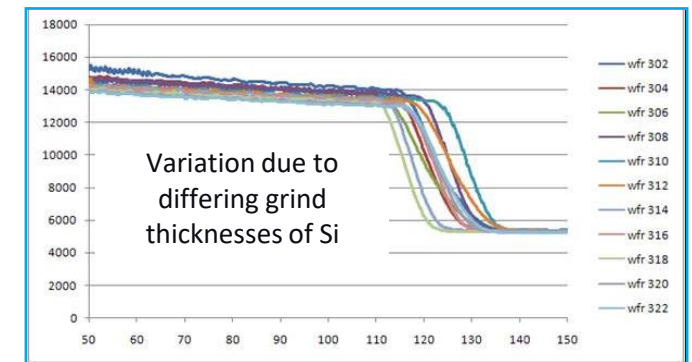


- Large operating envelope
- For all DRIE etches to a stop layer
- Detection limit <0.05% OA



**Etch Chamber**  
Rapid fluorination of SiF to SiF<sub>4</sub> Unable to 'see' SiF\*

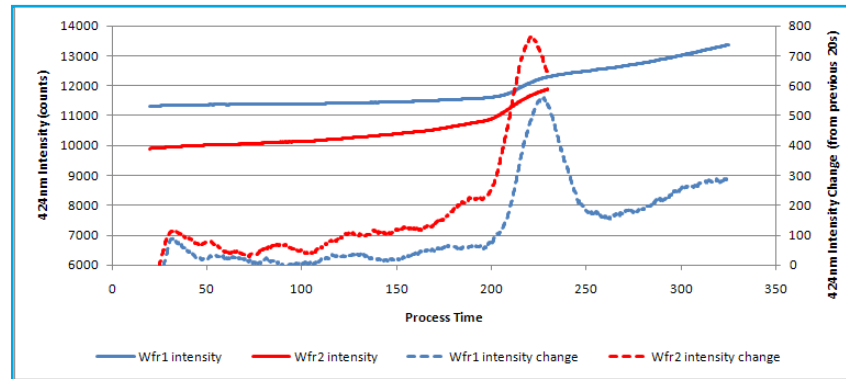
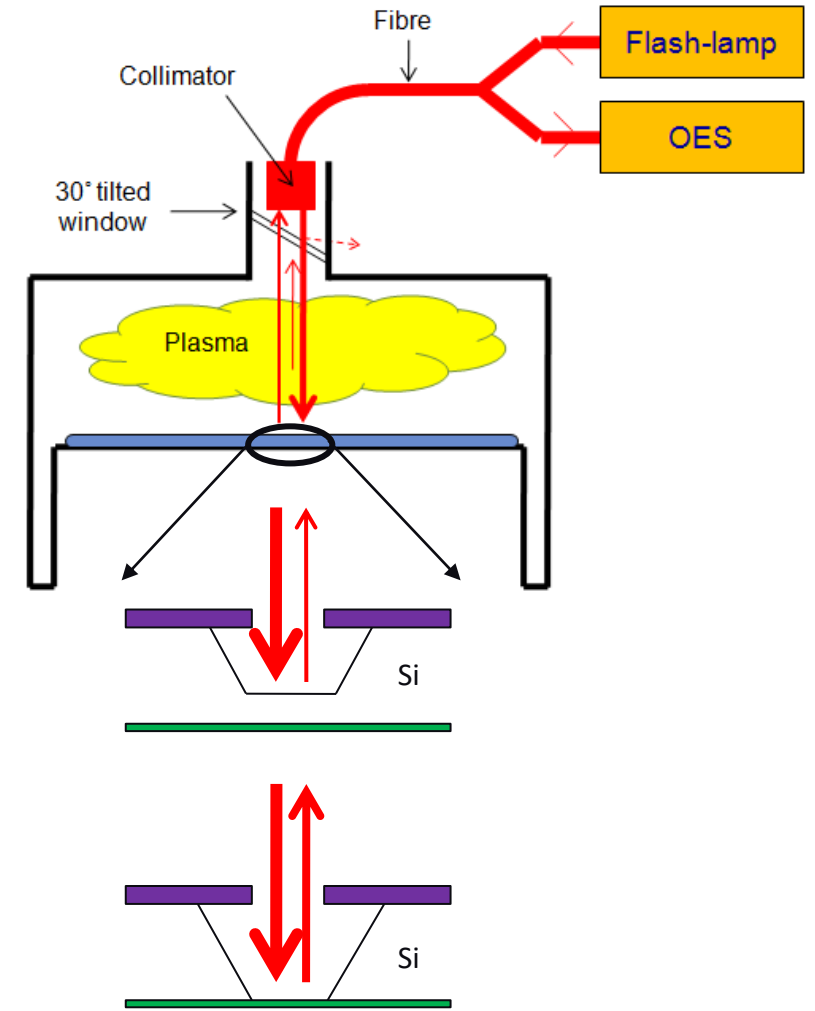
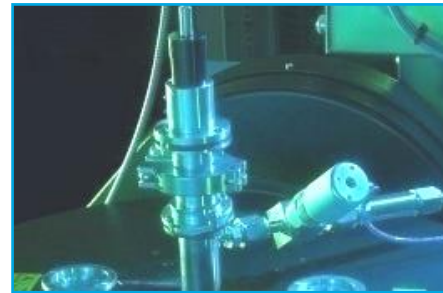
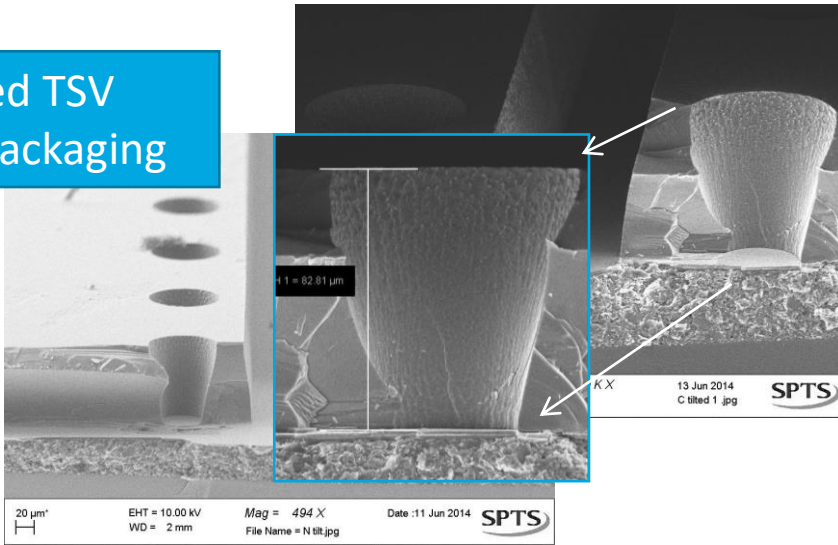
**Claritas Unit**  
High concentration of SiF<sub>4</sub> cracked to reform SiF\*  
Easily detected



# White Light Reflectance

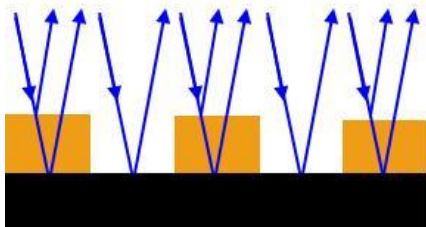
- In some cases there is no OES transition

Tapered TSV for Adv Packaging



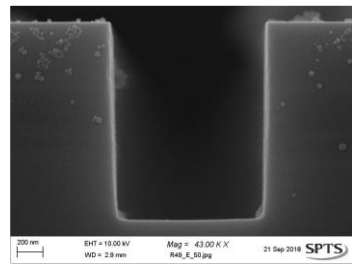
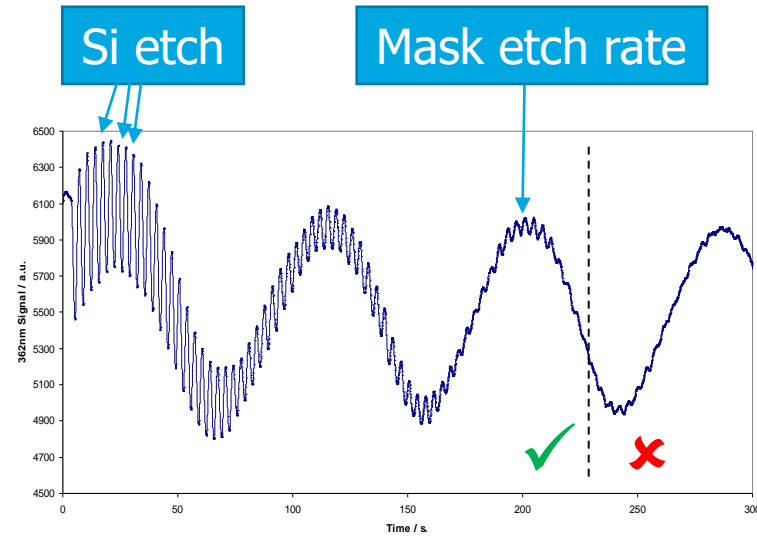
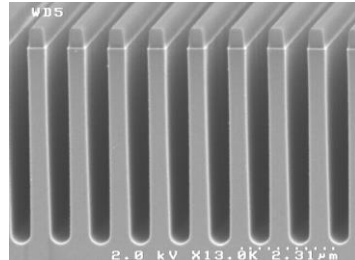
# White Light Interferometry

- Used for blind etches – no under-layer

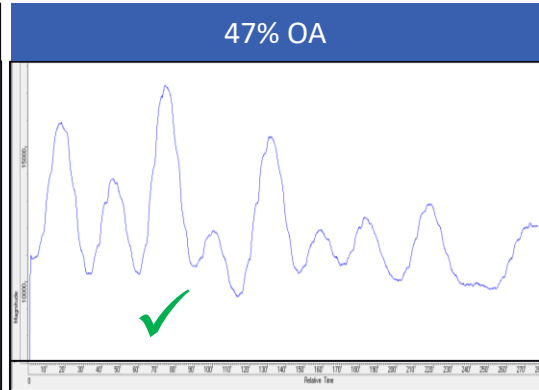
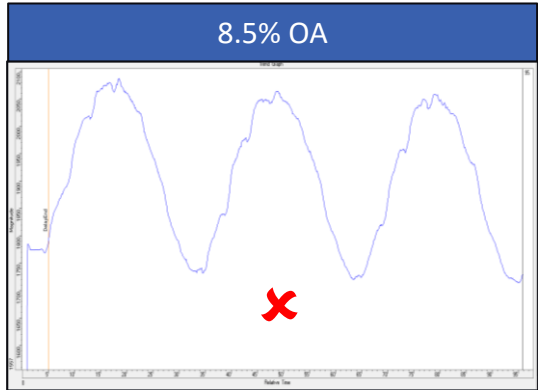


- ~2cm spot size means no requirement for dedicated feature on wafer
- Real time trench depth read-out on every wafer

Si trench etch for Power device

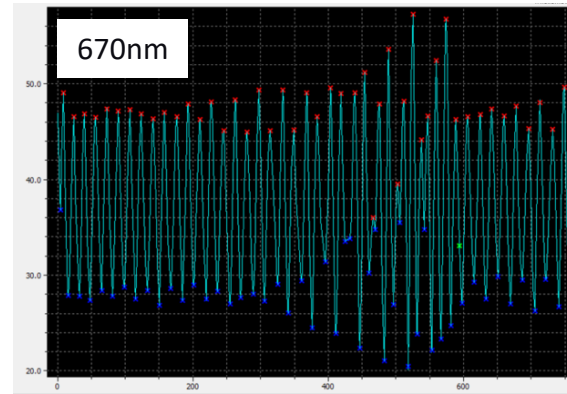
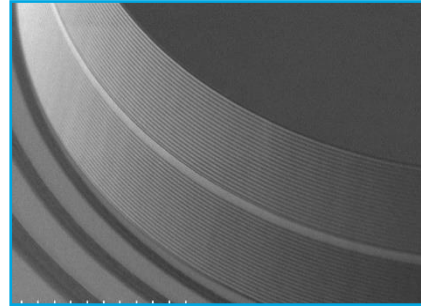


SiC trench etch for Power device

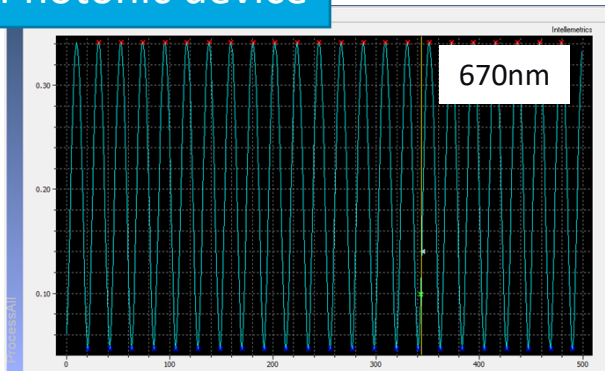


# Visible LASER Interferometry

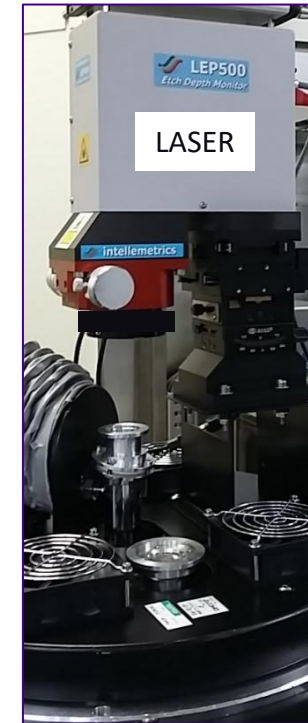
Mesa etch  
for VCSEL device



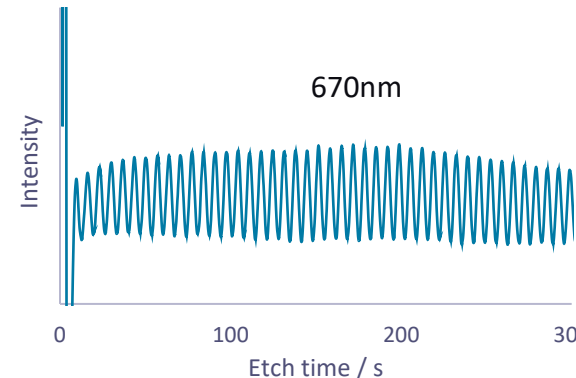
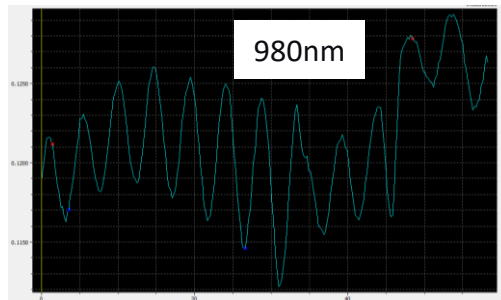
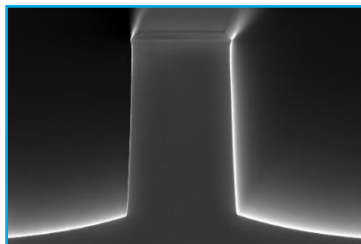
BCB blanket etch  
for Photonic device



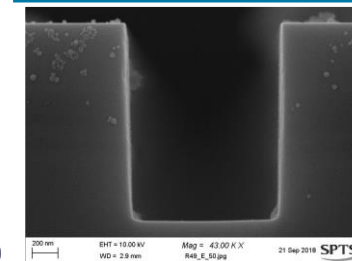
LASER spot  $\sim 20\mu\text{m}$  diameter  
Target 'window' typically required at  
wafer centre  
Wafer placement accuracy means  
window is  $300\text{-}350\mu\text{m}$  wide  
Optional Pattern Recognition software  
reduces window to  $100\text{-}250\mu\text{m}$



InP etch  
for Photonics device

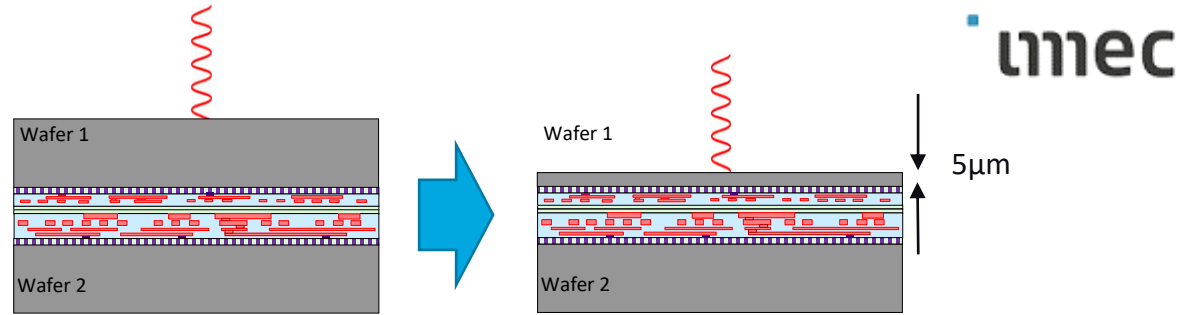


SiC trench etch  
for Power device



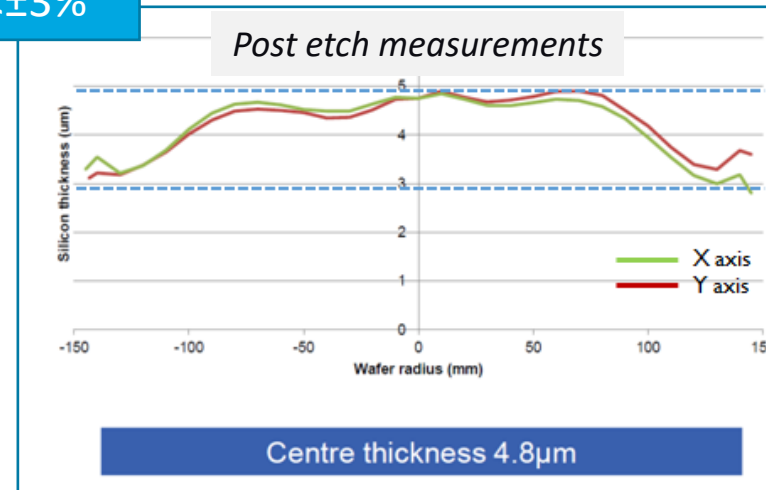
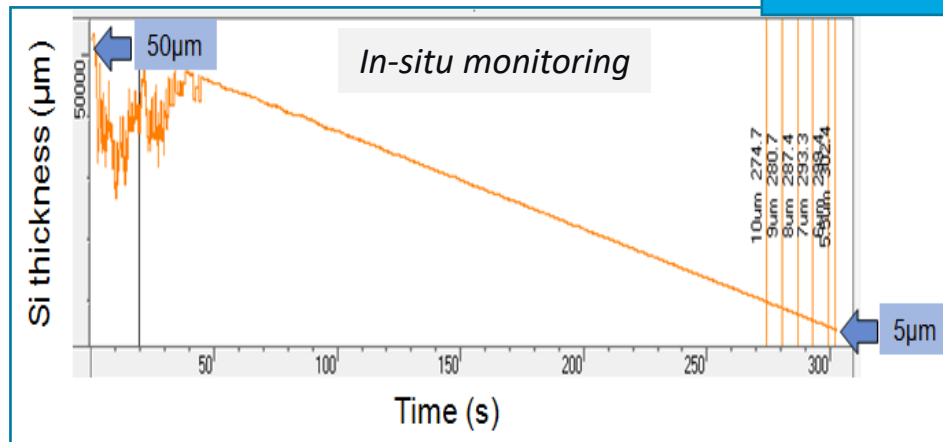
# NIR LASER Interferometry

Extreme Si thinning  
for Advanced Packaging



- Interferometry between front & back side faces of the Si
  - Semi-transparent in NIR (900-1700nm)
- Method correlates interference output with an optical model to compute thickness

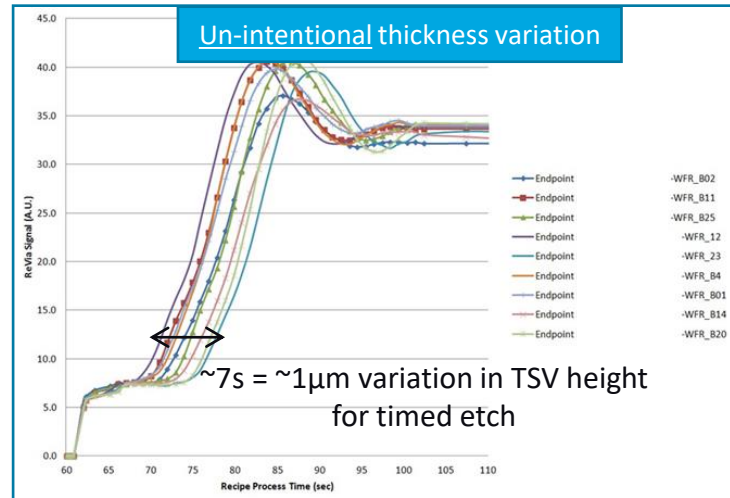
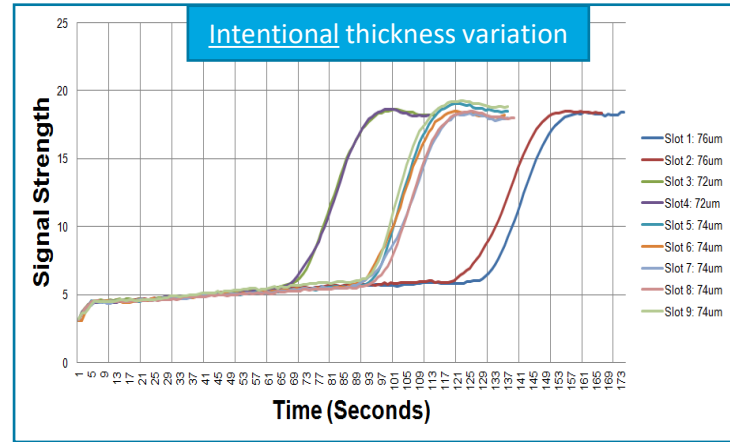
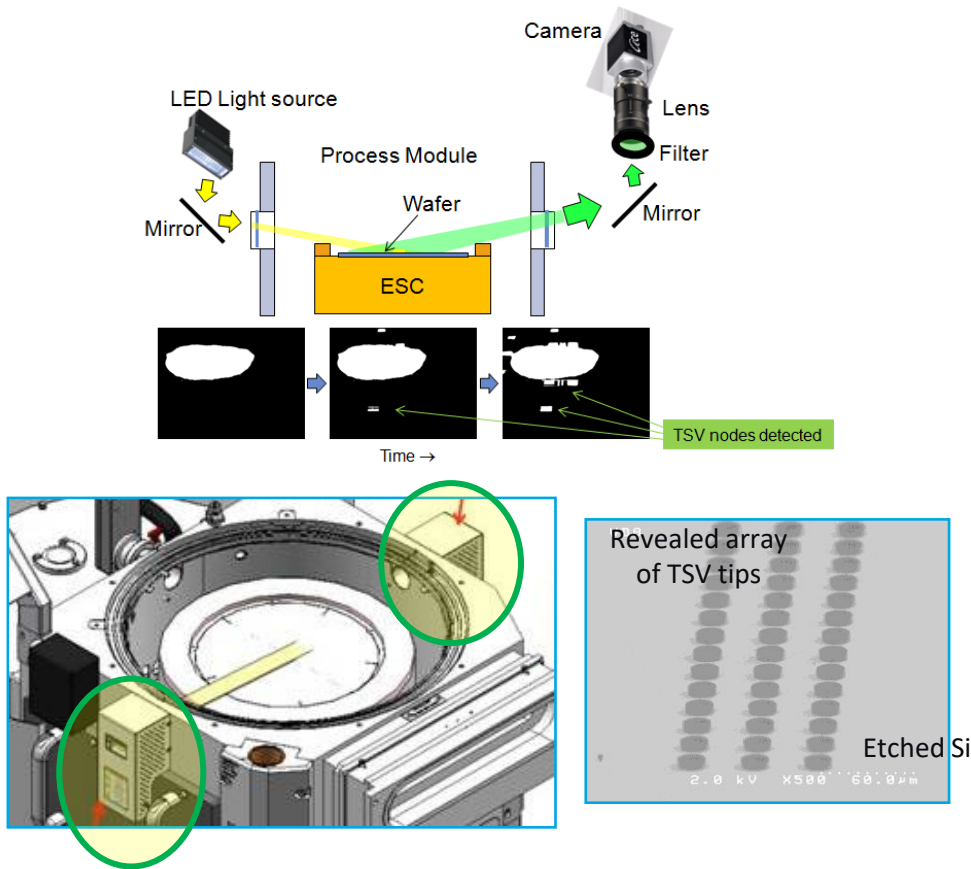
Etch rate >9µm/min  
Uniformity <±3%





# ReVia® (Patented)

- Accounting for incoming thickness variations = increased yield

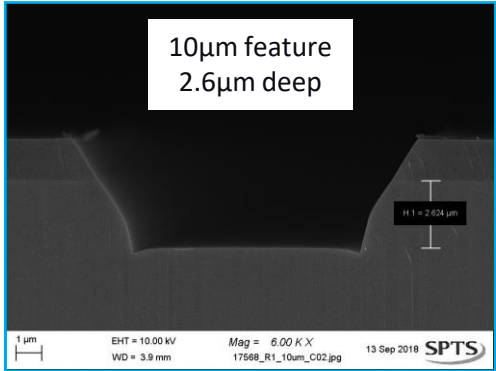


Unique & robust end-pointing for any TSV layout or RST variance

(10) Patent No.: US 8,709,268 B2  
 (45) Date of Patent: Apr. 29, 2014  
 (12) United States Patent  
 Ansell

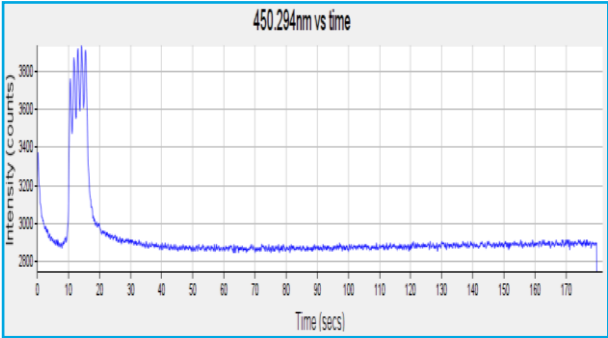
# Example of EPD Method Selection

- 350nm AlGaInN/2.3μm GaN
- Blind etch with no stop layer



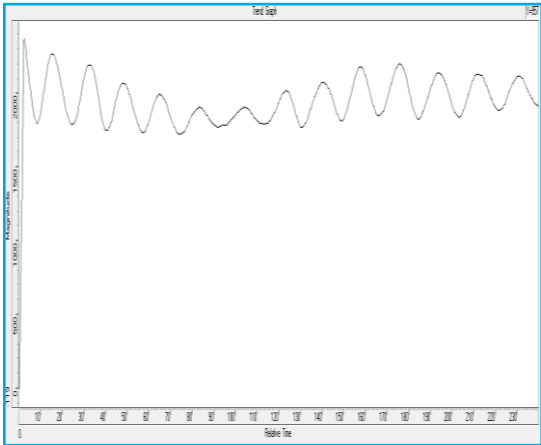
Multiple end-point systems can be applied to the same chamber (if required)

OES



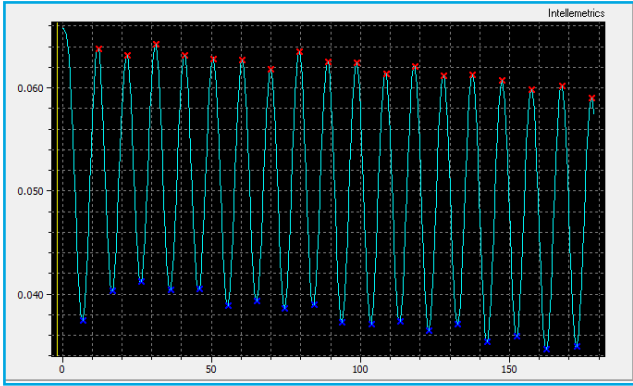
In\* used to detect layer transitions

WL interferometry



Weaker signal due to larger area  
Dual traces due to mask & GaN

LASER interferometry



Strong signal, small area, beam in a target feature  
No signal from mask



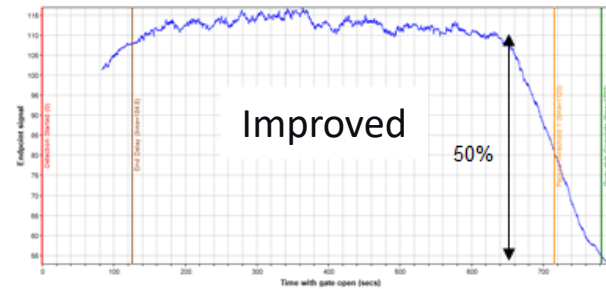
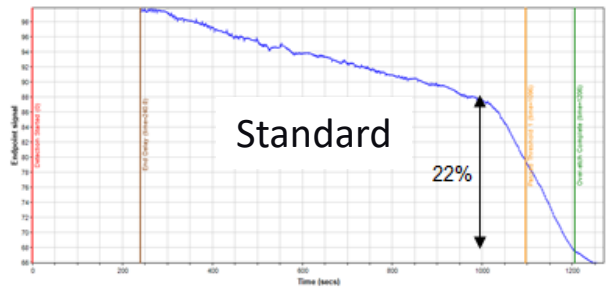
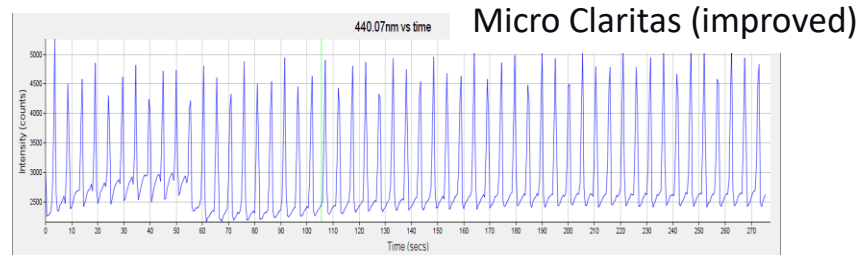
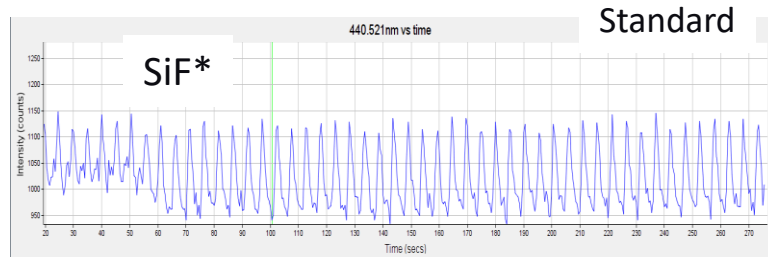
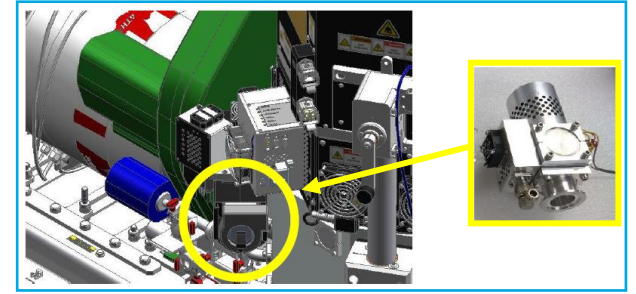
# End-point Detection Methods

Method	Monitors	Based on	Used for
Parametric*	<b>System</b>	APC angle He flow	Large open areas Through wafer etches
Optical emission spectroscopy (OES)	<b>Plasma</b>	Glow from plasma	General purpose when stop layer present (Poly, Oxide, Al, GaAs ...)
Claritas*		Re-ignited glow from plasma	Bosch Si etching
WL Reflectance*	<b>Wafer</b>	Reflection	Tapered TSVs
WL Interferometry		Broad area interferometry	Non-Bosch Si trenches SiC trenches
LASER interferometry		Small spot interferometry	VCSEL stacks SiC trenches
NIR*		Interferometry	Wafer thinning
ReVia*, Ascent*		Wafer vision	Via Reveal, SiC via etch

*\*Unique to SPTS*

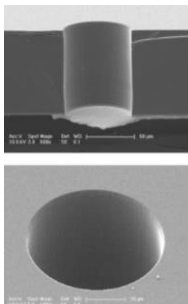
# NEW Developments

## Claritas™ improvements for Deep Si etching (*new* Micro Claritas™)

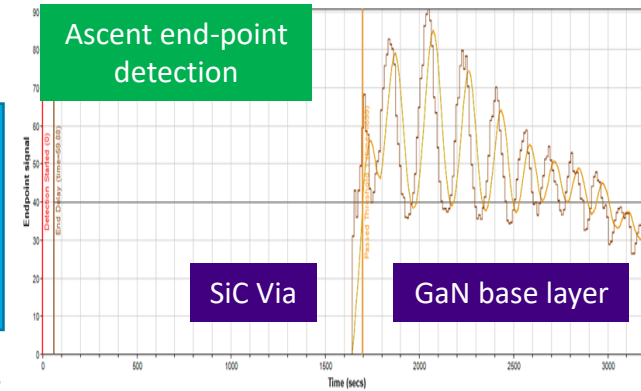


- Improvements in...
- Finer step resolution
  - Larger end-point change
  - **Field production validated!**

## SiC via etching (*new* Ascent™)



- Difficult for EPD because ...
- Low via density
  - Metal in plasma (from masking) reduces OES signals
  - **Success with new approach!**



Patent applied for

# Conclusions

- EPD is an essential tool for controlling Plasma Etching processes
  - Better devices & higher yields
- Datalogs, the plasma/gas or the wafer itself can be monitored *in-situ*
- Troublesome etches include very low OA%, high AR or blind features
- Solutions exist for a broad range of etches/device types
- SPTS has the broadest range of available methods
  - All fully integrated to the system software, multiple EPDs on the same chamber
  - Including unique methods such as ReVia<sup>®</sup> & Claritas<sup>™</sup>
  - Plus a new method for SiC vias! Ascent<sup>™</sup>
  - Contact us for more specifics for your applications and needs

# Web Resources @spts.com – Questions?

- Tech Insights

- <https://www.spts.com/resources/tech-insights>

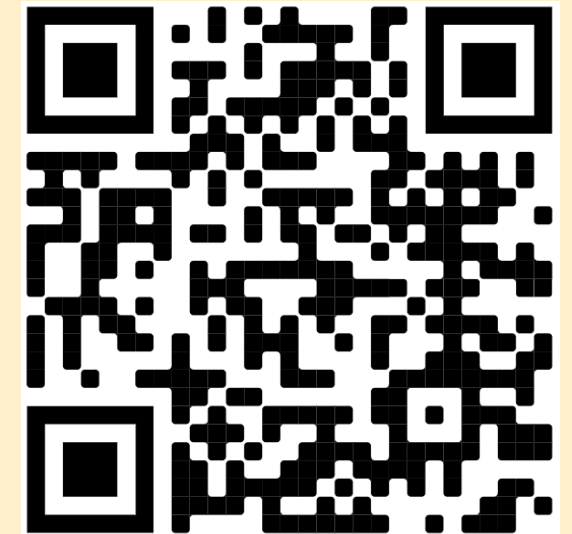


- Application Briefs

- <https://www.spts.com/resources/literature-library>

- Published Technical/Conference Papers

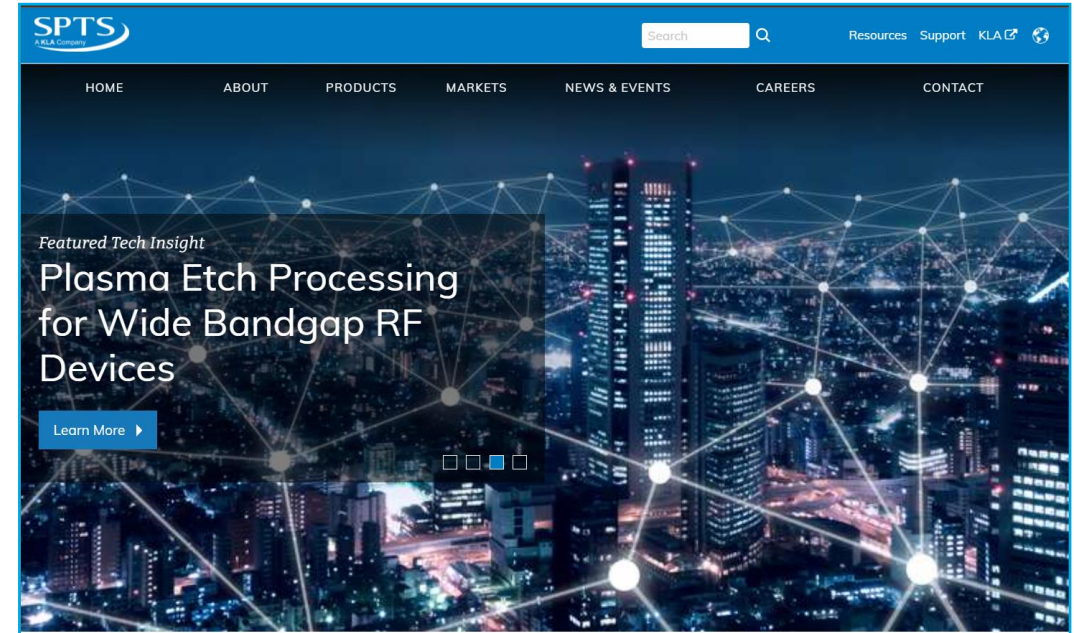
- <https://www.spts.com/resources/presentations>



# Thank you!

## More Questions?

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