Fabrication of Nanoscale Silicon Membranes on SOI Wafers Using Photolithography and Selective Etching Techniques:

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Introduction

- ASU building compact hard x-ray free-electron laser
- Smaller and less expensive than current models
- Hard x-rays with ultra-short pulses do not damage tissues
- Able to image living molecules in-situ
- Future use in medical research and green energy development

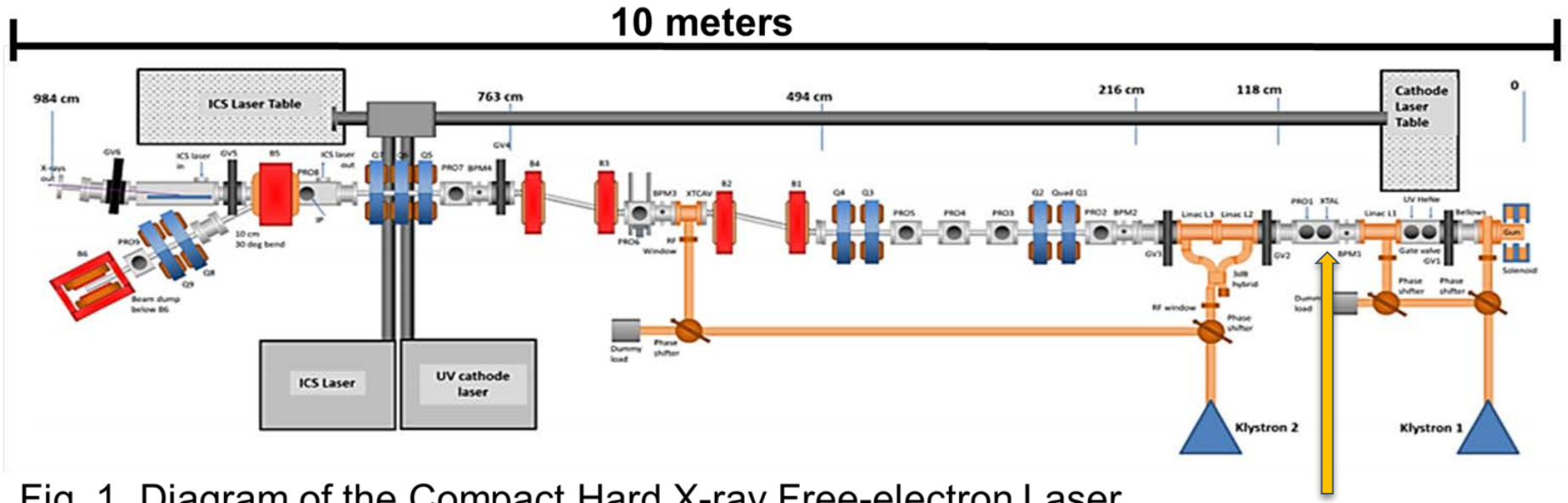


Fig. 1. Diagram of the Compact Hard X-ray Free-electron Laser.
Nanni, et. al. 2018

Diffraction Crystal Here

Project Objectives

- Create Free-Standing Silicon Membranes
  - Acts as base for electron diffraction grating in laser

- Develop Photolithography and Etch Processes
  - Use silicon on insulator (SOI) wafers with 220 nanometer silicon membrane layer

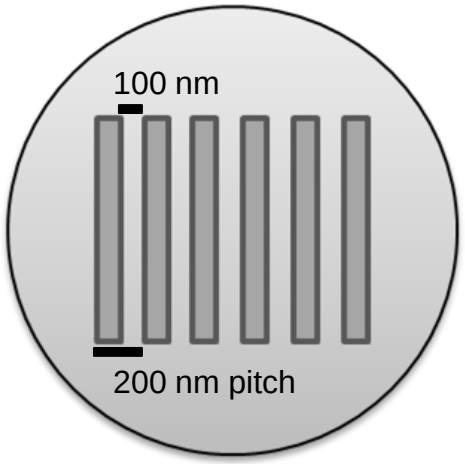


Fig 2. Plan View of Grating in Membrane

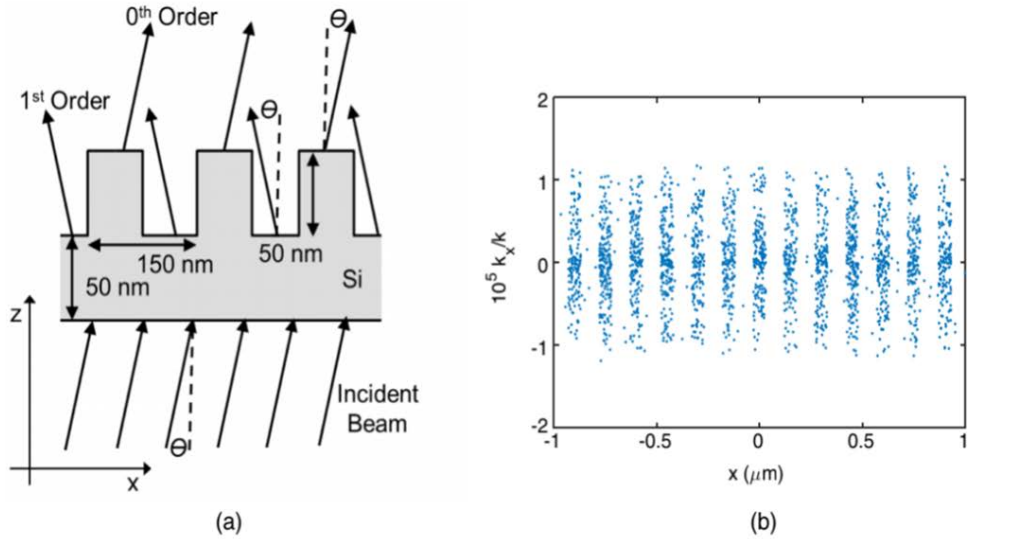


Fig. 3. Diffraction Grating Cross-section (a) and Modeled Forward-scattered Pattern of the Electron Beam (b)
Nanni et.al, 2018

Process Flow

Back: Bulk Silicon 675 microns

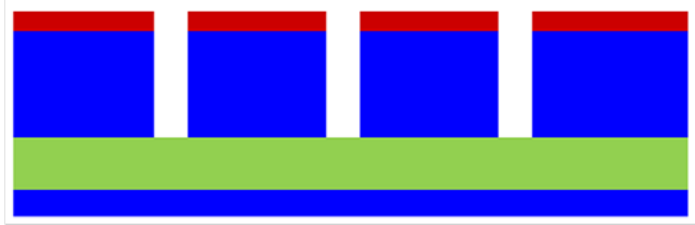
Buried Oxide 3 microns

Front: Silicon Membrane 220 nm

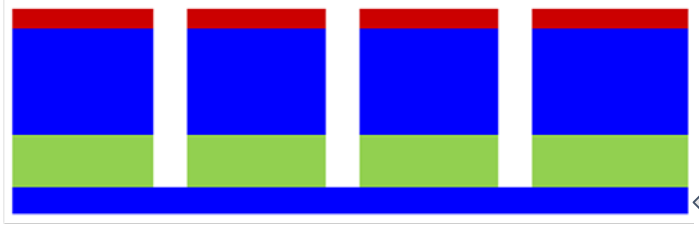
1. Silicon on Insulator (SOI) Wafer, 2D cross-section

2. Spin-coat Photoresist (PR) on Back

3 & 4. Expose and Develop Pattern



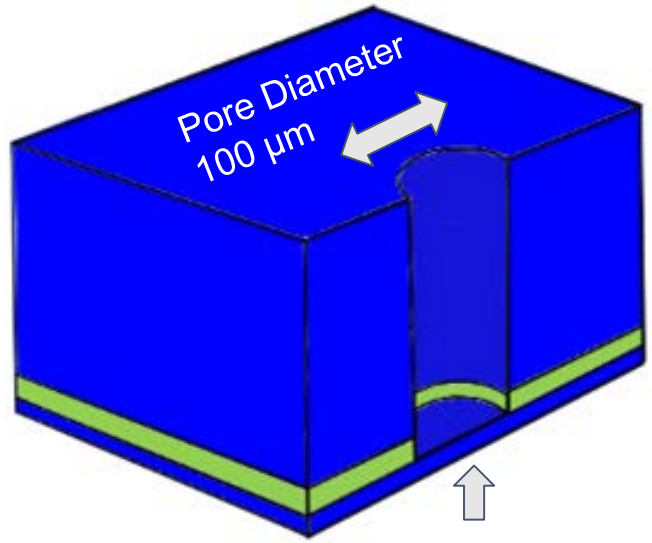
5. Plasma Etch Bulk Silicon



6. HF Etch of Buried Oxide

Silicon Membrane 220 nm

Fig 4. 2D Cross-section of Process Flow in SOI Wafer



Silicon 675 µm

Buried Oxide 3 µm

Silicon Membrane 220 nm

Fig 5. 3D Cross-section of Pore in SOI Wafer

Photolithography on Polished Si, 1

- Deep etch (675 micron) requires thick PR layer
- Approx 1 micron PR lost per 67 microns Si etch depth
- Need 12 - 13 microns of PR to complete full etch
- Spin curves from manufacturer not accurate to our conditions and equipment
- Created our own Spin Curve by testing PR thickness with various spin speeds in-house

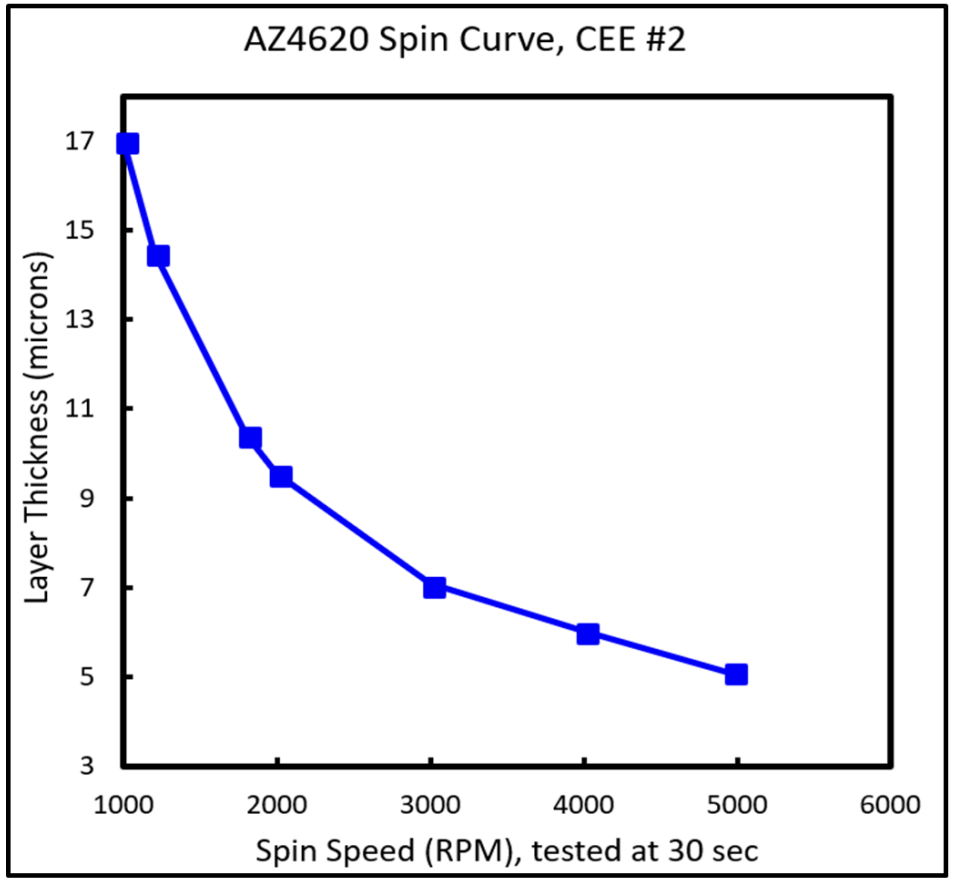


Fig. 6. Photoresist (PR) Spin Curve

Photolithography on Polished Si, 2

- Able to clear thick resist layers
- Developed pores are clean
- Target pore diameter = 100 microns

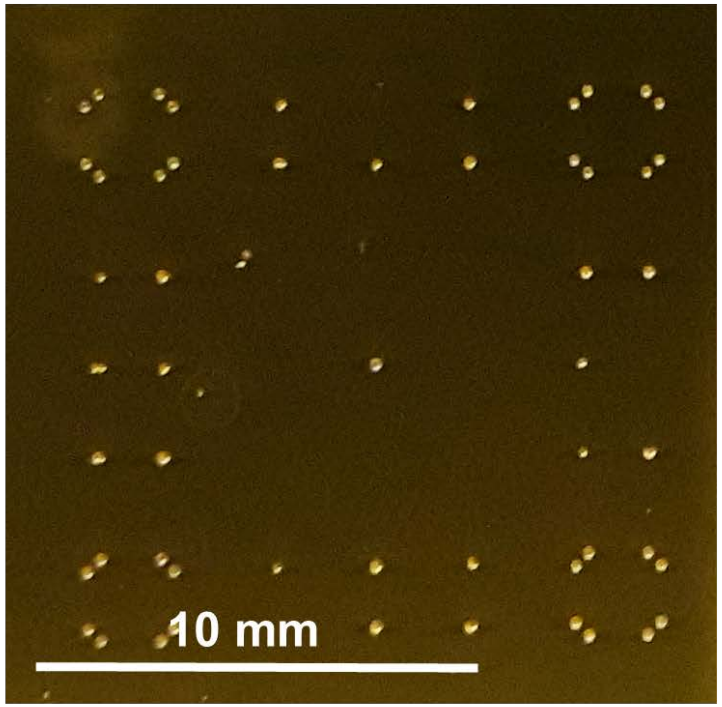


Fig 7. Developed Pattern

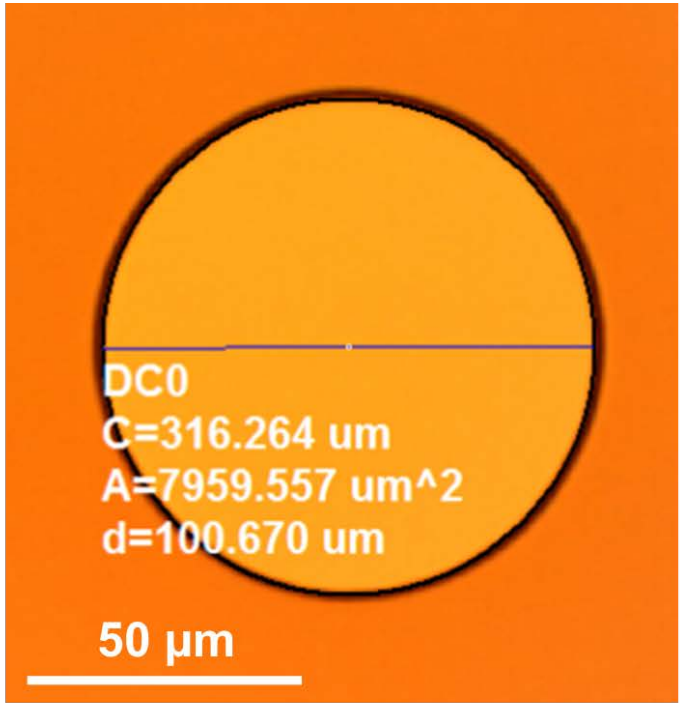


Fig 8. Developed Central Pore

Etching on Polished Si

- Test etch on polished Si practice wafer
- Obtained etch rate and Si etch:PR loss ratio

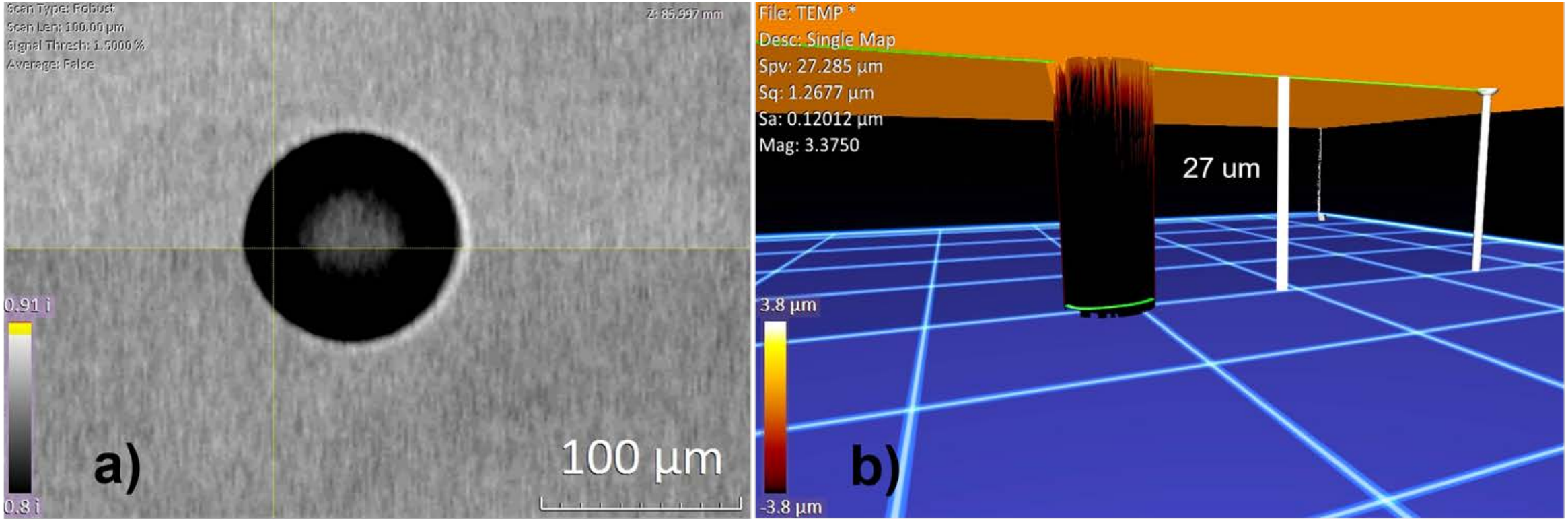


Fig 9. a) Overhead Image and b) 3D Profile of Etch Test on Polished Si. Taken with Zygo Profilometer

Photolithography on Unpolished SOI

- Process consistent on polished Si
- Began work on SOI wafer
- Rough, unpolished backside presented challenges
- Pattern development not clean
- Result not good for etching

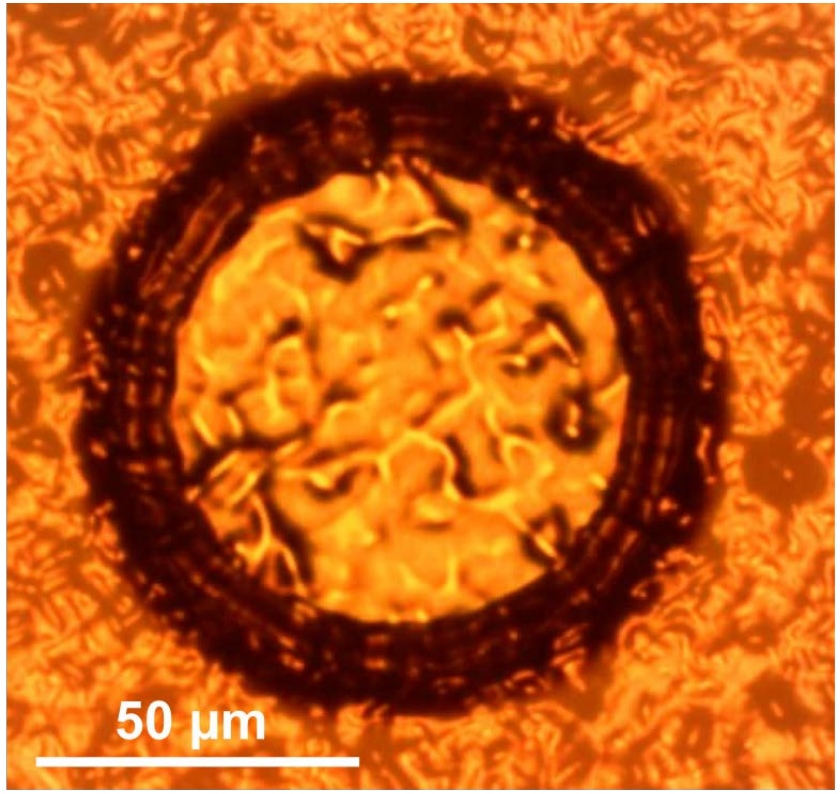


Fig 10. Developed Pore on Unpolished Backside of SOI

Developed Pore on Polished Si (for comparison)

Etching on Unpolished SOI

- Didn't have time to redo photo process
- Used a different mask for etch test
- New pores several mm square, rather than 100 micron round
- Etch produced a membrane, but separated and slid off pore
- Stress too much for 220 nm silicon membrane to handle

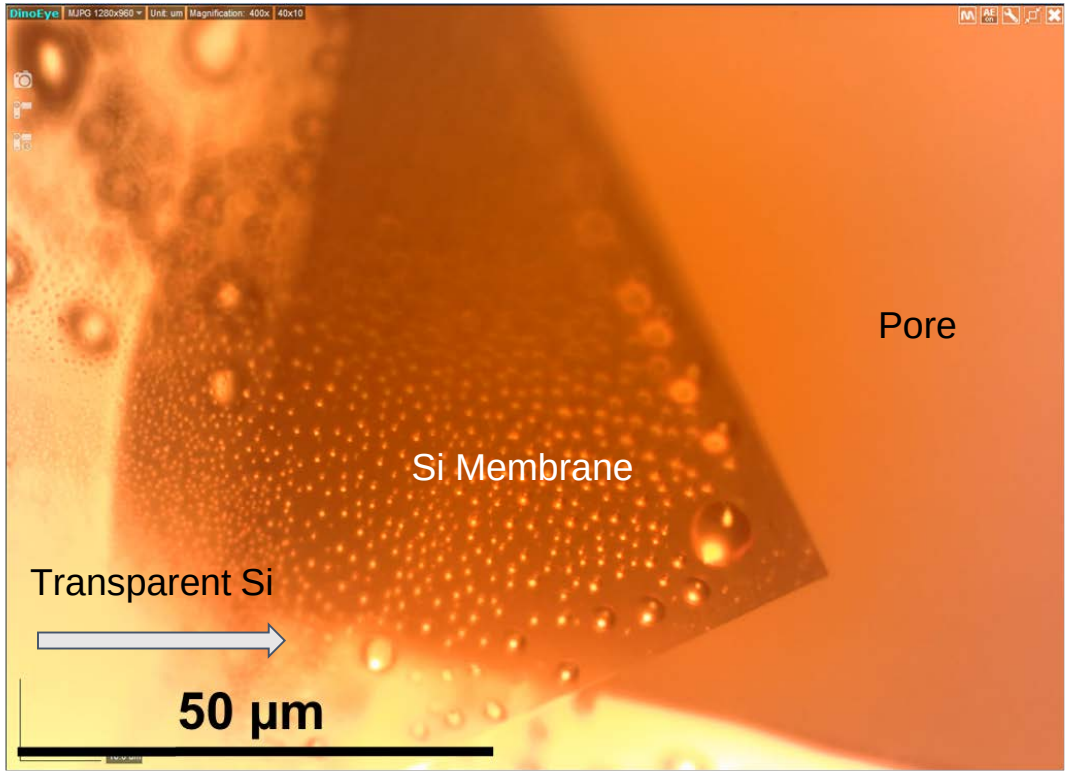


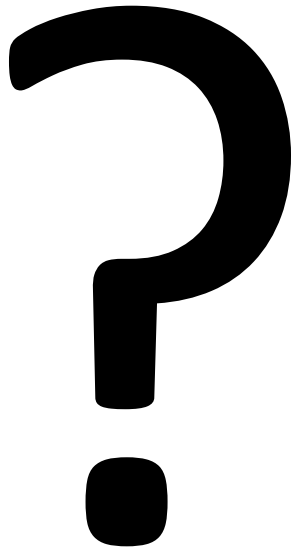
Fig 11. Fully Processed Pore with Separated Membrane Sitting on SOI Front side

Conclusion

- Developed Good Process for Polished Silicon Pieces
- Unpolished Backside of SOI Wafer Presented Challenges
- Able to Etch SOI after Removal of Oxide Layer (> 1 µm) on Back
- Larger (square) Pore Size Used on SOI Caused Membrane Separation due to Stress
- SOI Process Needs Refining
- For Optimal Results, Start with SOI Wafers Polished on Both Sides (Double Polished)

References:
E. A. Nanni, W. S. Graves, and D. E. Moncton. Phys. Rev. Accel. Beams 21, 014401 – Published 19 January 2018

Questions?



PR Thickness with F40 Microscope

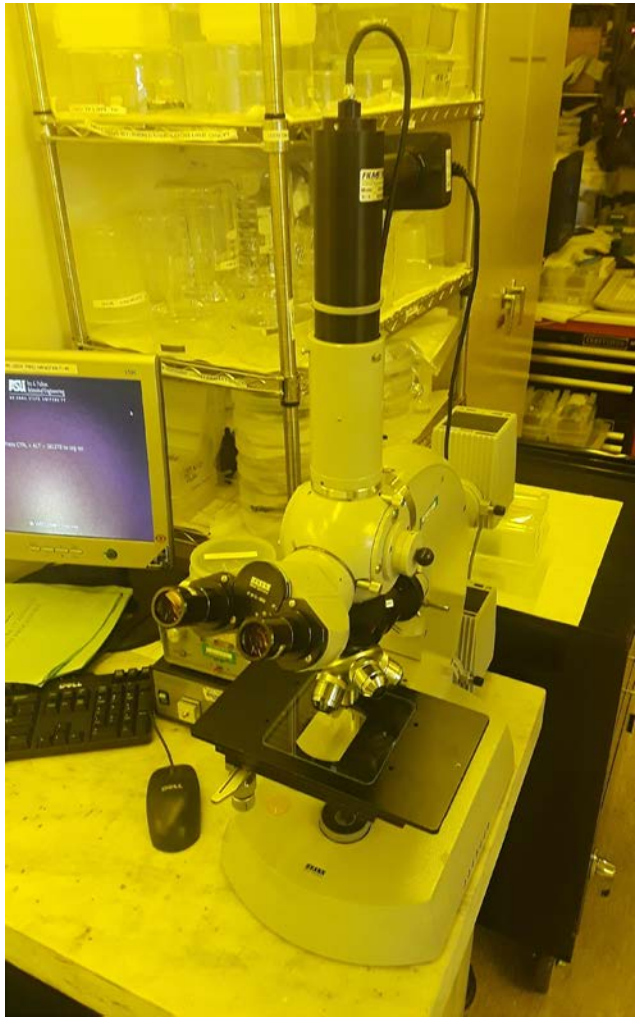


Fig 14. F40 Microscope

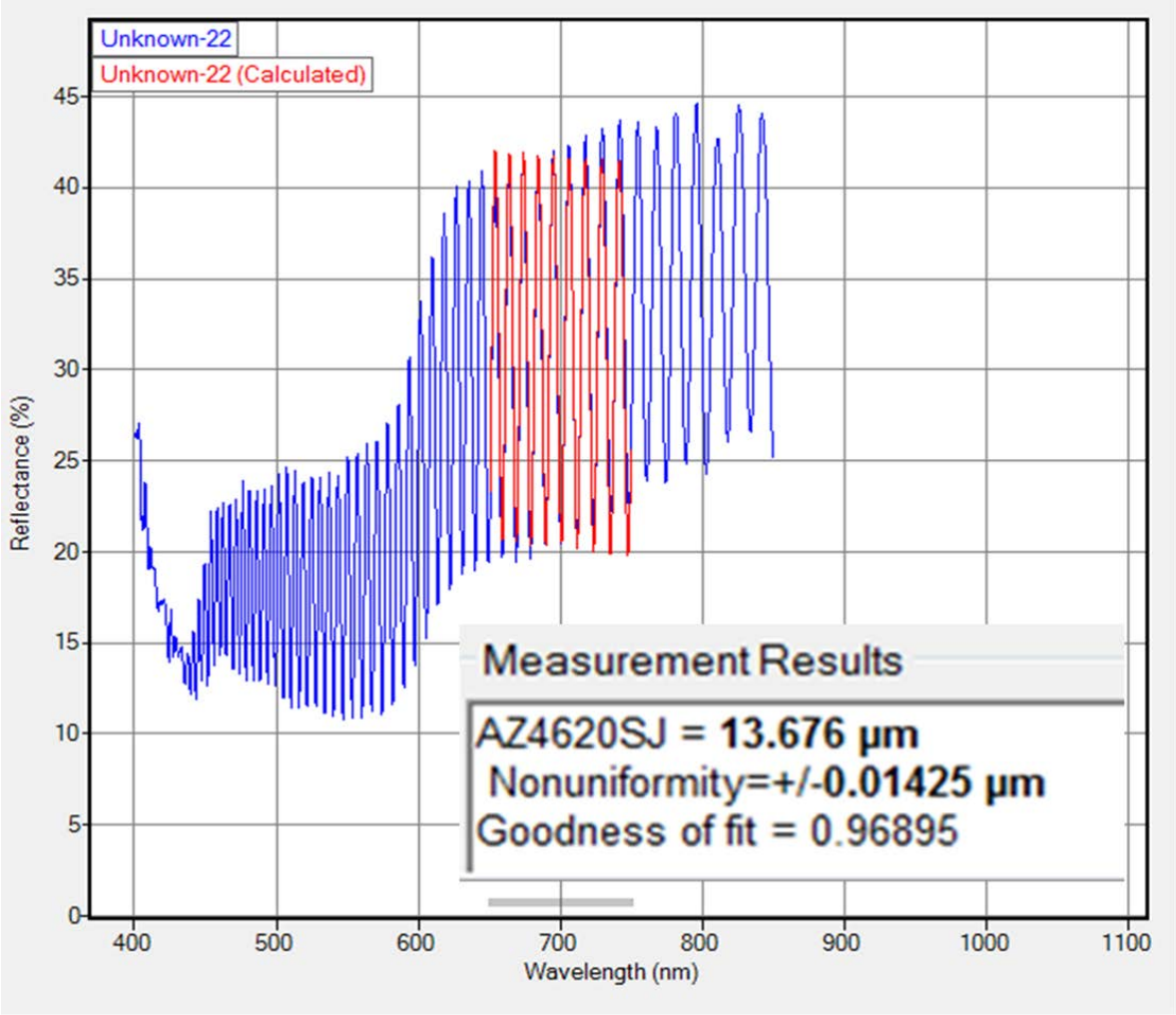


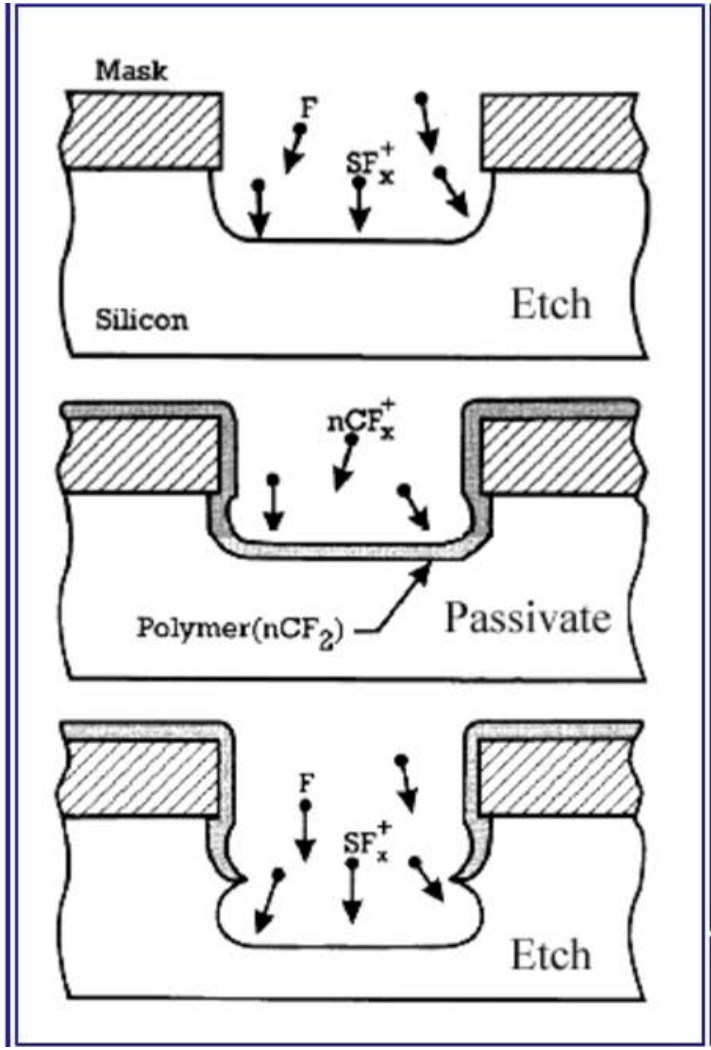
Fig 15. PR Thickness Calculated from F40 Reflectance Measurement

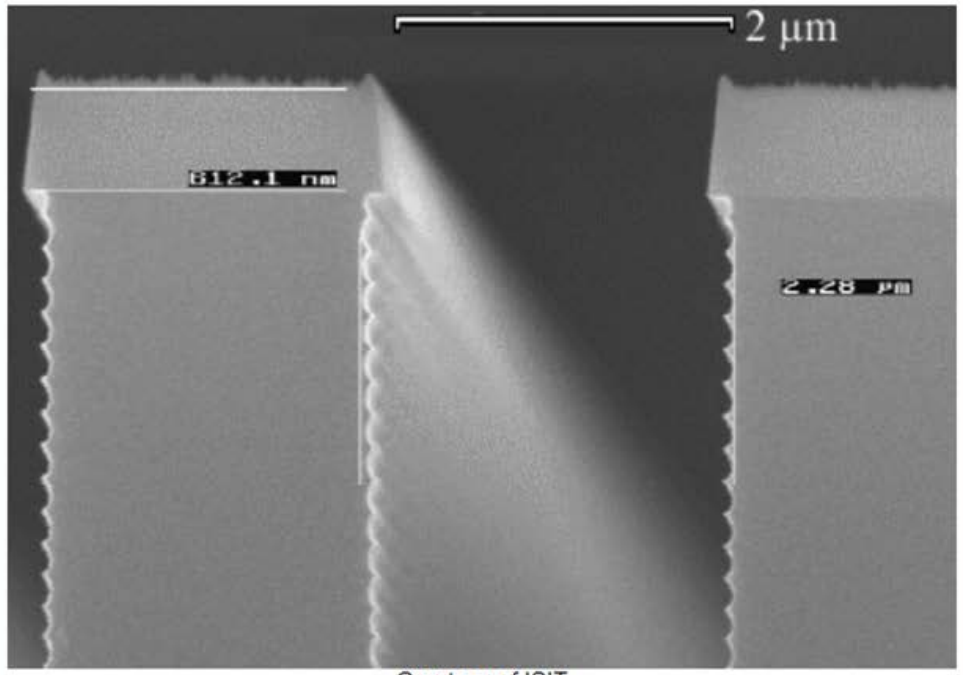
- Enter Materials
- Est. Thickness
- Take Reflectance
- GOF > 0.9
- Software calculates actual layer thickness
- Repeat multiple times over wafer area and take average

Note: On Graph,
Blue is Estimated, and
Red is Calculated

STS Plasma etching, Bosch Process

Fig 12. STS DRIE Plasma Etcher





Courtesy of ISIT

The ***scalloped*** shape is typical for the Bosch process.

Fig 13. Example of Bosch etching process. Picture courtesy of © H. Föll (Semiconductor Technology - Script)

Machines Used During Process

Equipment used, shown in order of Process flow

Fig 16. Cee Spinner, F40 Microscope, EVG620 Mask Aligner, Development Bay, STS Plasma Etcher

WHY SILICON?

Si is common and inexpensive

Easy to etch and fabricate

Atomic structure gives desired electron beam diffraction