National Nanotechnology
Coordinated Infrastructure

LOW TEMPERATURE PLASMA TECHNOLOGIES FOR ADVANCED PACKAGING APPLICATIONS

OUTLINE

- Plasma-Therm Introduction
- Deep Silicon Etching / TSV
- Strip / Clean / Surface Modification
- TSV Liners / Barriers / Seeds
- ICP Deposition
- Plasma Dicing

LONG HISTORY OF INNOVATION AND GROWTH

1974 – **Founding**
RF power supplies

1983 – Industry 1st single wafer production plasma etch reactor

1994 – 1st Photomask plasma etch system introduced

2000 – unaxis oerlikon
Acquired by Oerlikon

2009 – Plasma-Therm
Spun Out
Headquarters in FL

2010 – **Established**: Critical machining
REV-TECH MANUFACTURING SOLUTIONS

2011 – ADVANCED VACUUM A Plasma-Therm Company
Acquired: R&D line

2013 – **Released**: Industry 1st plasma dicing on tape

2015 – nanoplas
Acquired: HDRF

2016 – Plasma dicing Global Sales & Service Partner
DISCO

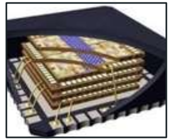
2018 – Nano Etch Systems Incorporated
CORIAL A Plasma-Therm Company
KOBUS
Acquired: BE, IBD, F.A.S.T.

2020 – **Acquired**
PVD, RTP, IBE, IBD
JLS Designs Limited
OEM GROUP

Nearly 50 years | 85,000 sq. feet, | International presence
Manufacturing – Class 1000 | Application/Demo – Class 100
Manufacture to Order

VLSIresearch RANKED 1st SUPPLIERS Customer Satisfaction 2020
20+Years
Customer recognition

Advanced Packaging | Wireless & Connectivity | Sensors & MEMS | Photonics | Memory Data Storage | Power | R&D



Etch

ICP – High Density
RIE – Low Density
DSE™ – Deep Reactive Ion Etch
IBE – Ion Beam
Low Damage

Deposition

PECVD
HDPCVD
PVD
IBD – Ion Beam Dep
F.A.S.T. – Fast Atomic Sequential Technology

Material Modification

HDRF – High Density Radical Flux

RTP – Rapid Thermal Processing

Dicing (Die Singulaltion)

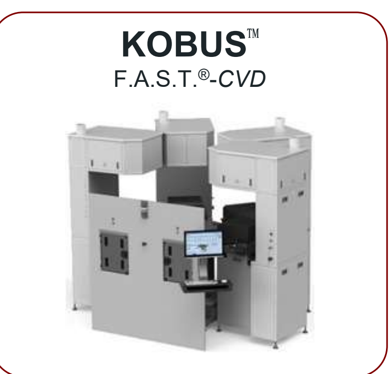
PDOT– Plasma Dicing Tape

Plasma Dicing on Wafer

TECHNOLOGY, PROCESS & PRODUCT INNOVATION

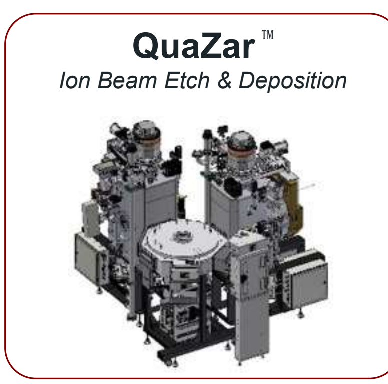
VERSALINE®
Etch & Deposition

KOBUS™
F.A.S.T.®-CVD



SINGULATOR®
Plasma dicing

QuaZar™
Ion Beam Etch & Deposition



ENDEAVOR & ECLIPSE
Sputter Deposition

Etch, Deposition, Material Modification & Dicing Technologies

KAYEN / ODYSSEY™
Stripping & Cleaning

CORIAL
Small footprint for R&D

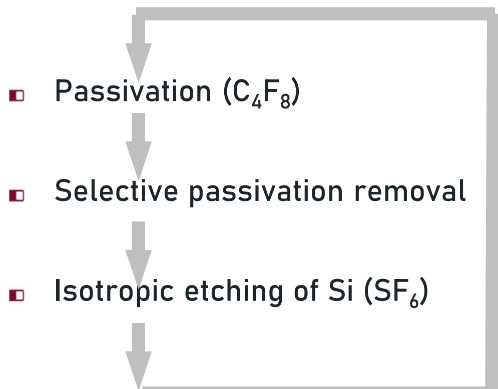
LAPECVD™
Deposition

TEGAL & HEATPULSE
Etch & RTP

MASK ETCHER®
0.5 um to EUV

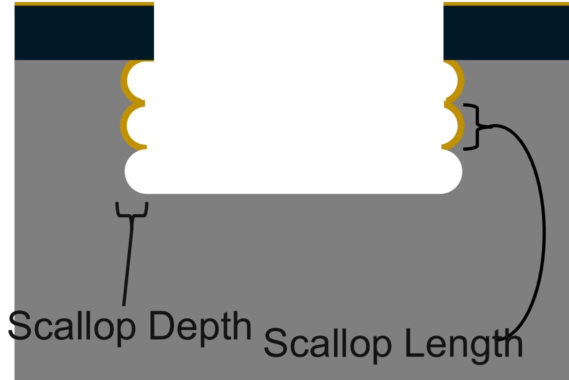
Deep Silicon Reactive Etching

- Cyclical process



- Passivation (C_4F_8)
- Selective passivation removal
- Isotropic etching of Si (SF_6)

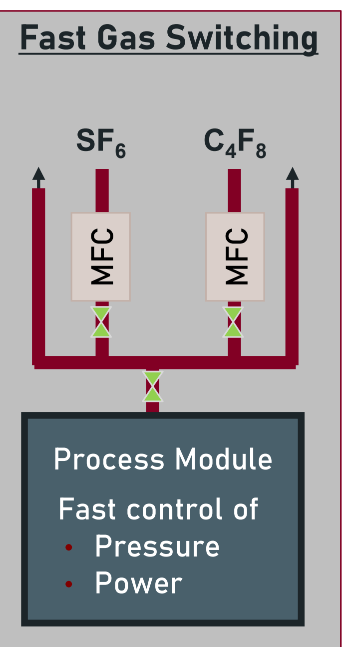
- Low temperature <20C
- High material selectivities (>250:1 to PR, >700:1 to SiO_2)
- Vertical

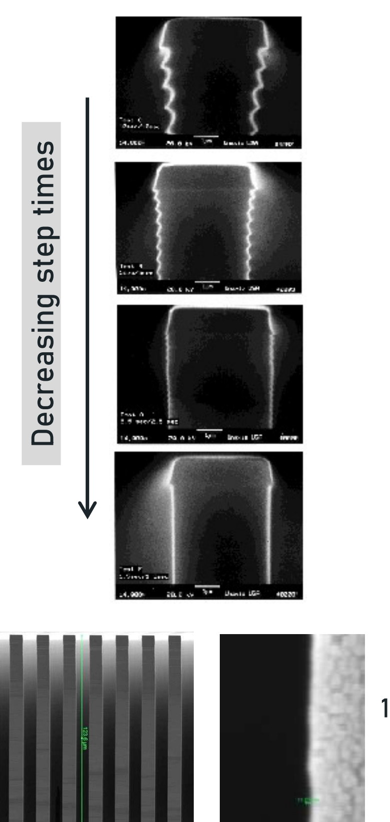


Also known as Bosch or Time Division Multiplexing (TDM)

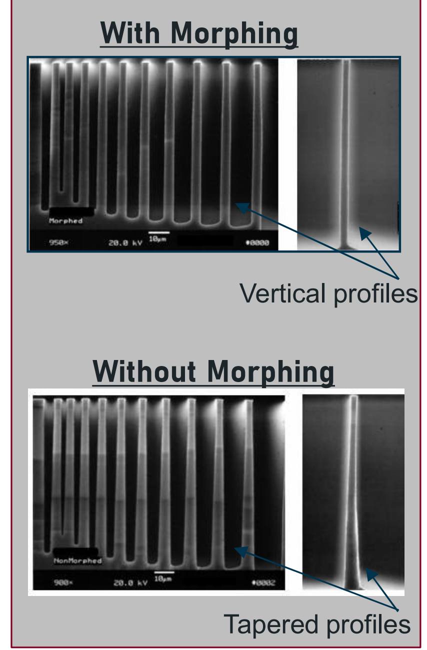
FAST PROCESS STEPS AND DETAILED PROCESS CONTROL

Low scalloping

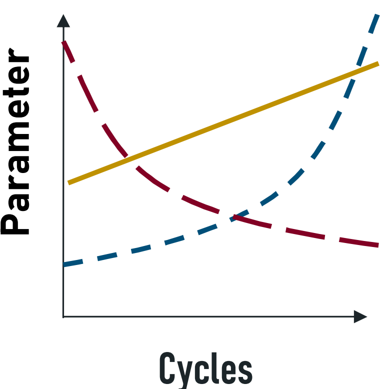




Profile Control

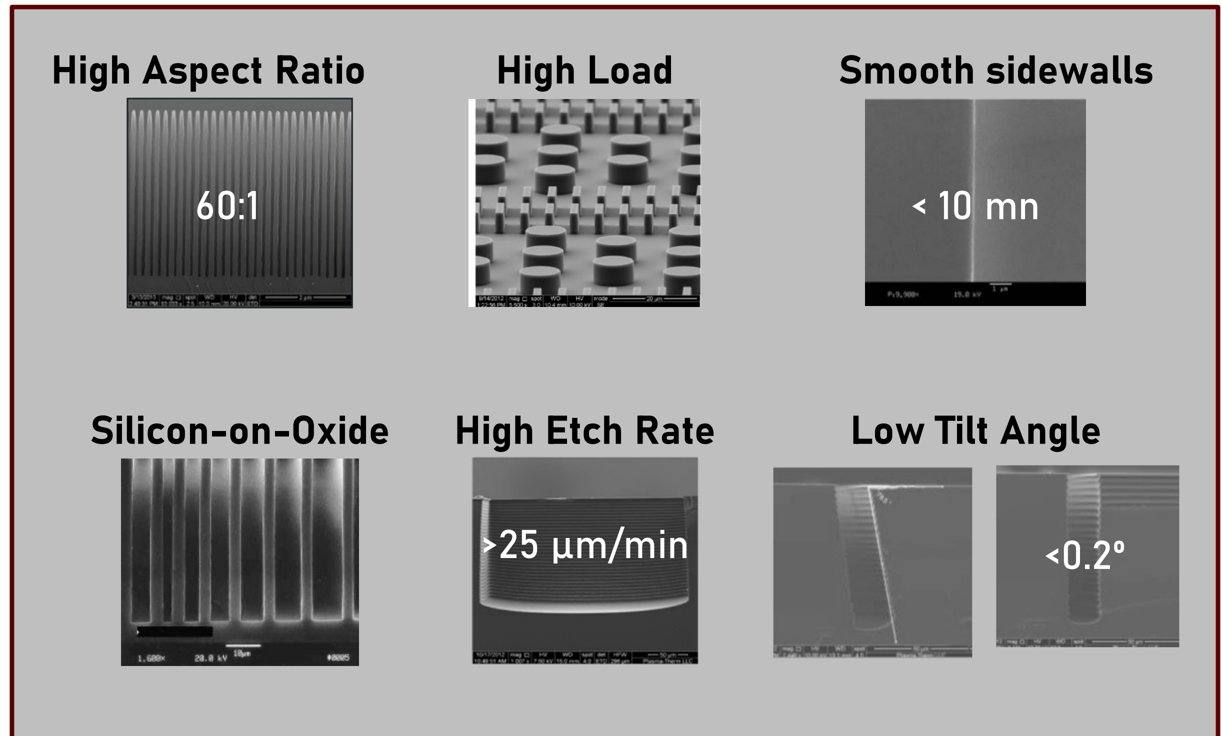


Parameter	*start*	*end*	*path*
Bias (V)	375	550	0.2
Dep time (sec)	1.5	3	2

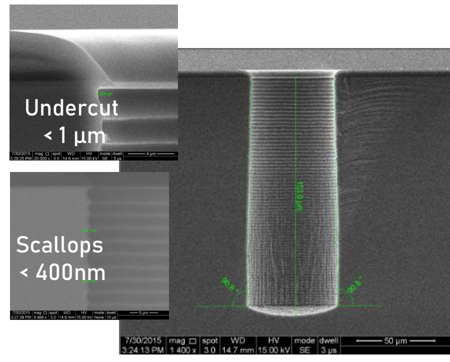


Adjustable Parameter
Rate of Change

WIDE RANGE OF APPLICATIONS

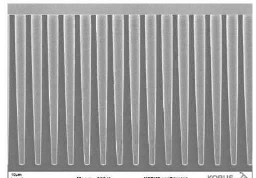


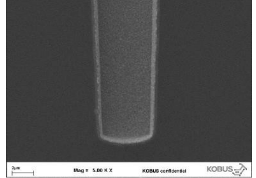
50µm Via diameter
400µm deep



High rate

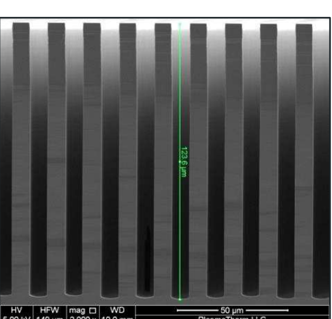
10µm Via diameter
100µm deep





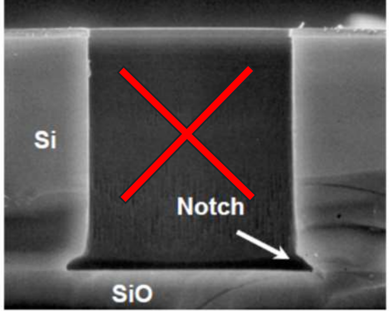
Tapered profile

8µm Via diameter
120µm deep

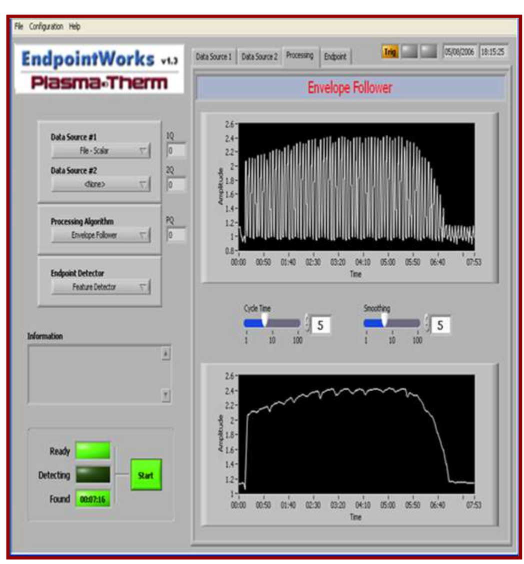


Vertical profile

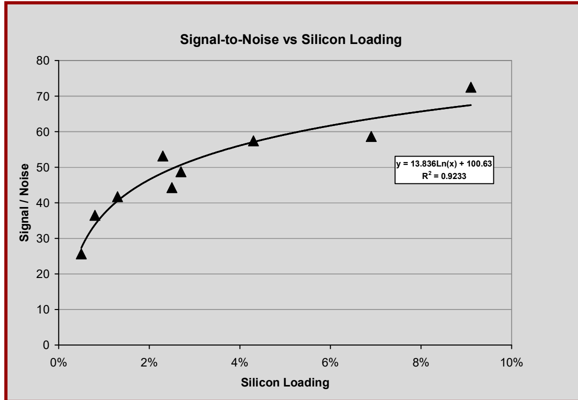
SENSITIVE OES ENDPOINT DETECTION FOR SOI

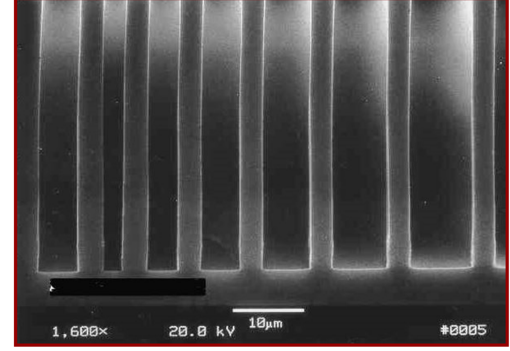


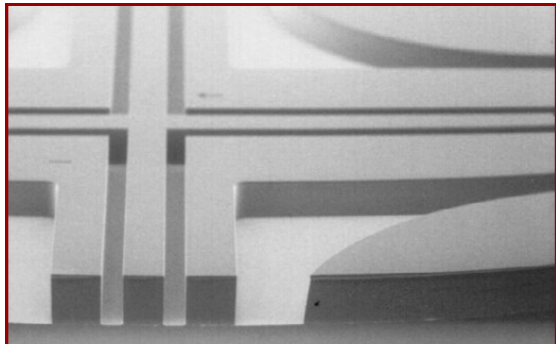
Cyclical signal: Changing gases, pressures, powers

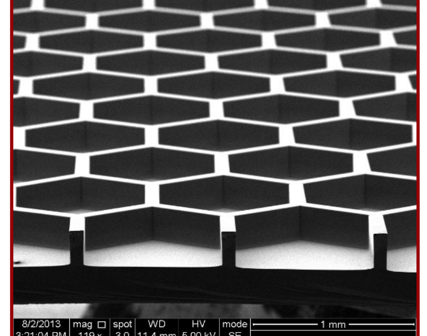


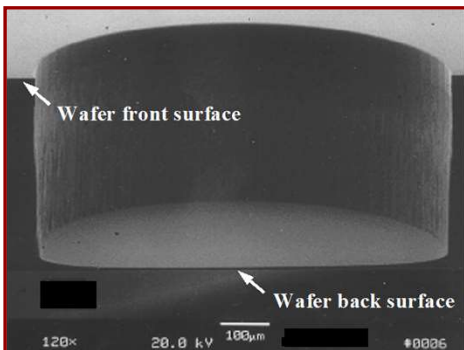
High sensitivityto oxide
<1% open area





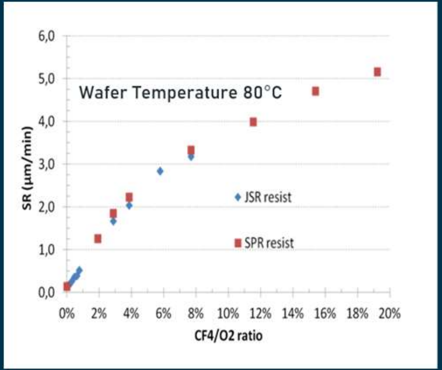






No Undercut at
Si/SiO_2 Interfaces

Low Temperature Strip / Clean / Surface Modification

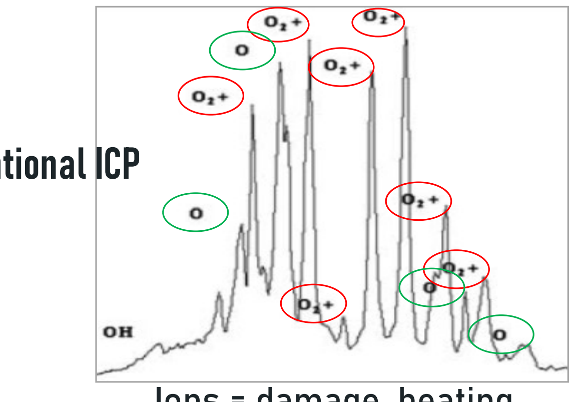


HDRF Distributed "mini" ICPs

Baffle
Ions
O* radicals
Wafer
Vacuum

Active species: O* + Ions

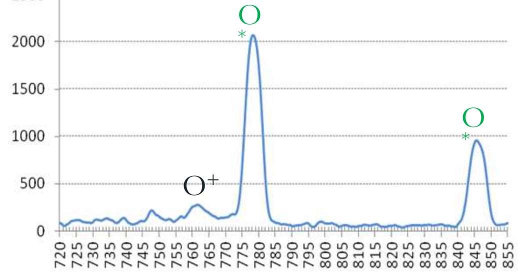
Conventional ICP



Ions = damage, heating

Active species: O* Radicals

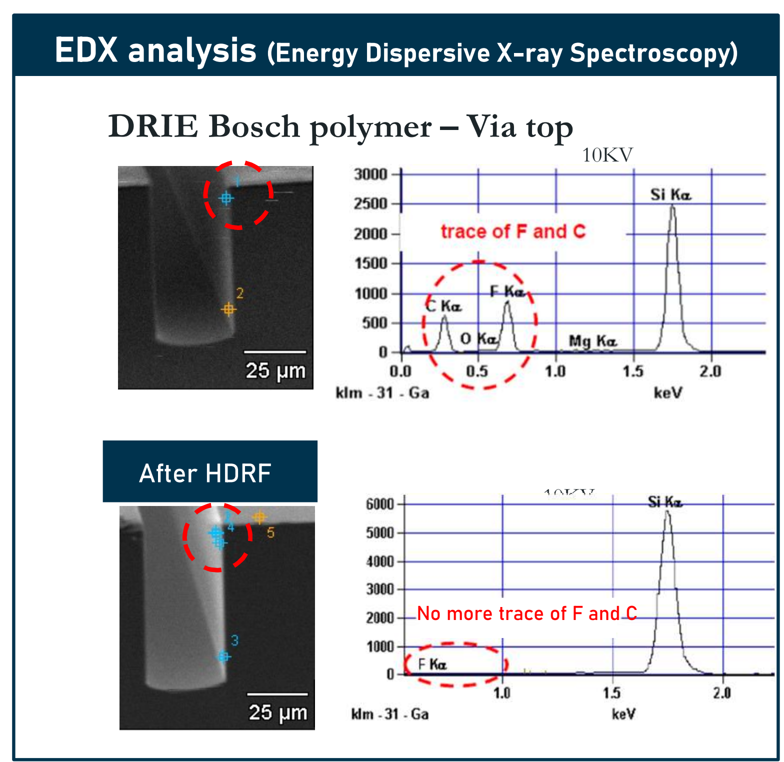
HDRF

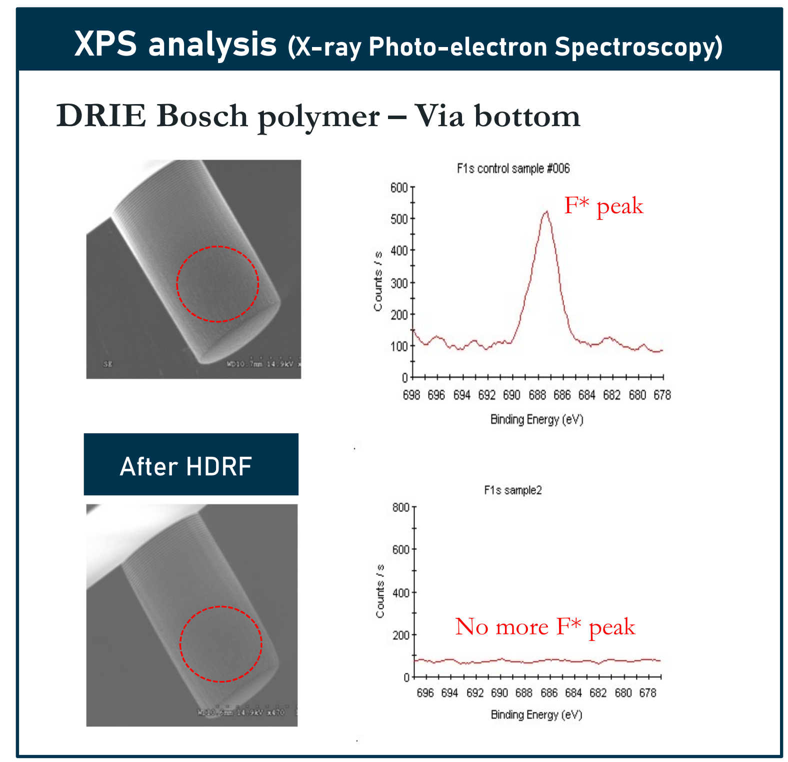


High plasma density ICP source

- Radical density > 1E17 cm^{-3}
- Mainly O* radicals at wafer level
- Low ions at wafer level
- Low temperature processing <80°C

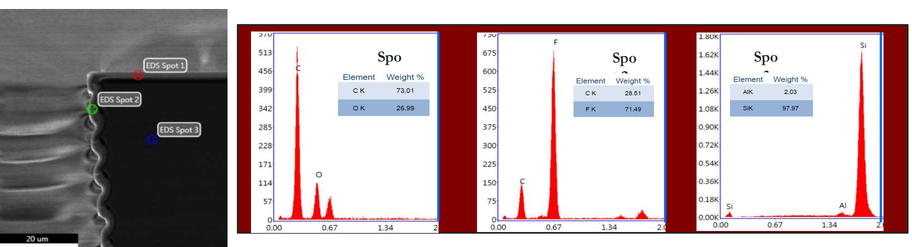
- **Low impact to sensitive devices**





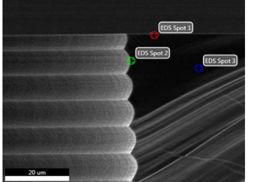
Efficient dry cleaning technology, to remove fluoro-carbon polymers

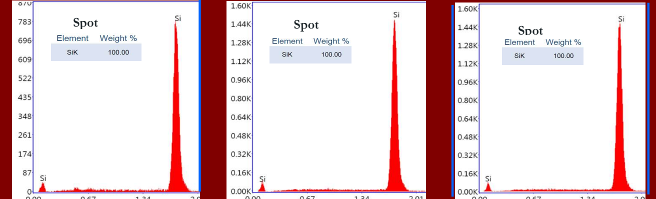
PR & POLYMER REMOVAL

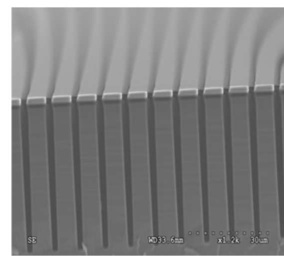


EDAX

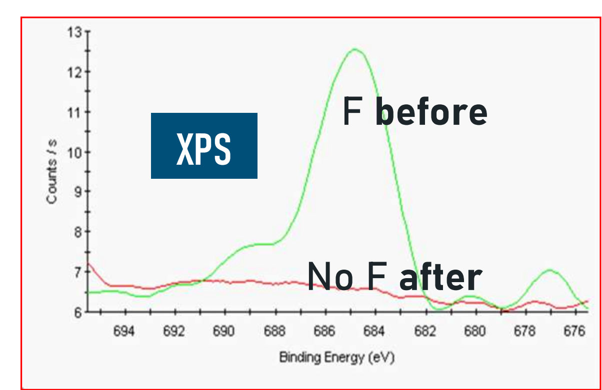
	C (Weight %)	O (Weight %)	F (Weight %)	Si (Weight %)
Spot 1 (PR)	73 → **0**	27 → **0**	0 → **0**	0 → **0**
Spot 2 (polymer)	29 → **0**	0 → **0**	71 → **0**	0 → **0**
Spot 3 (baseline)	0 → **0**	0 → **0**	0 → **0**	98 → **100**

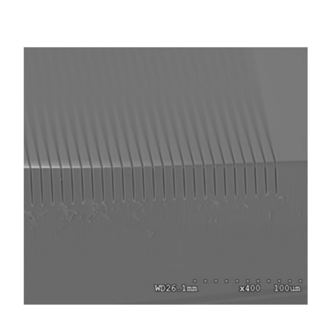






Before clean

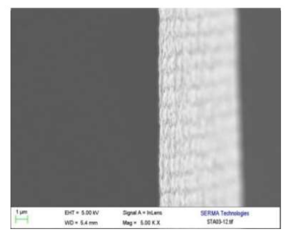
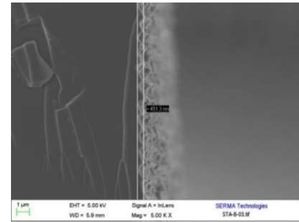
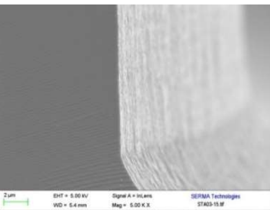




After clean

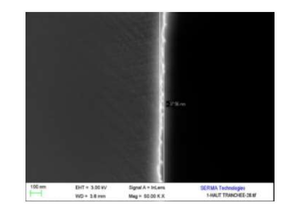
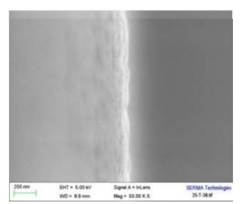
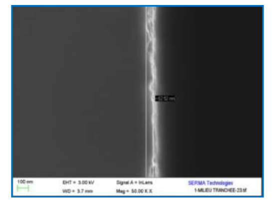
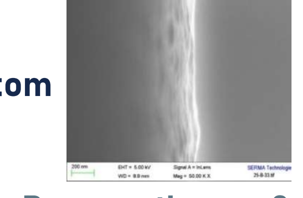
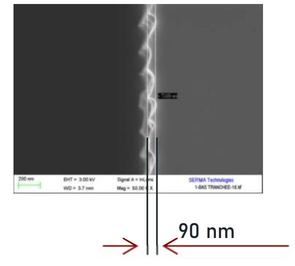
SCALLOP SMOOTHING DRIE STRUCTURES

Low Aspect Ratio (0.5:1)

	Before **HDRF** treatment	After **HDRF®** Smoothing
Top Scallop 380nm		
Bottom Scallop 490nm		

No more scallop in big cavity

High Aspect Ratio (30:1)

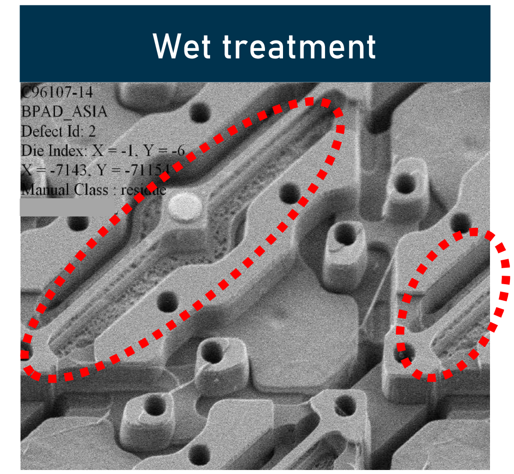
Before **HDRF®** treatment		After **HDRF®** Smoothing
	**Top**	
	**Middle**	
	**Bottom**	

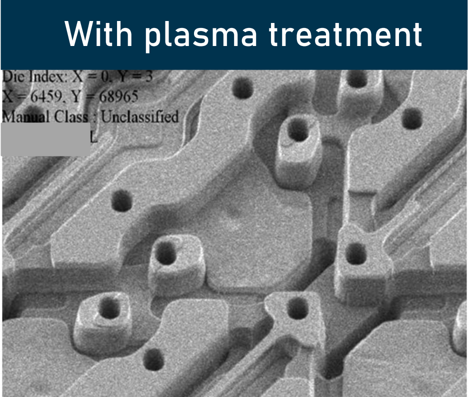
90 nm

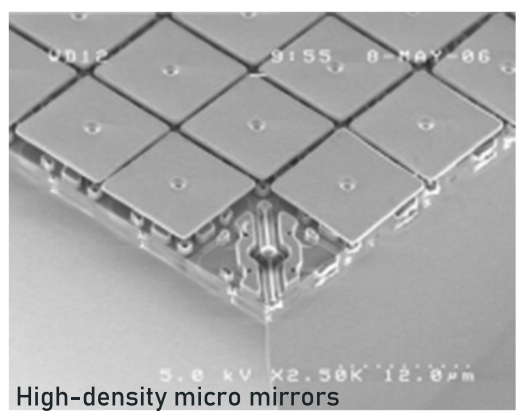
Process time : < 2 minutes

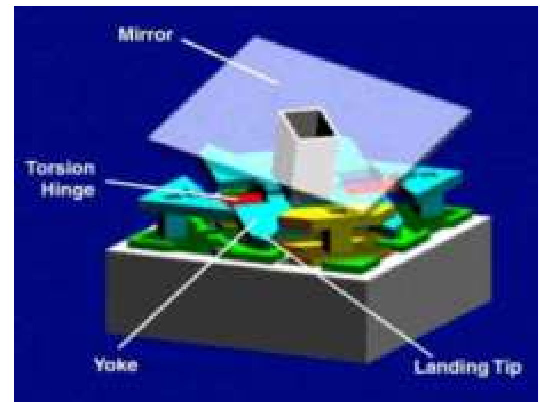
-> CD loss ~3% in narrow trench

- Elimination of mirror tilt due to residues
- Damage-free. No electrical charging
- Yield improvement





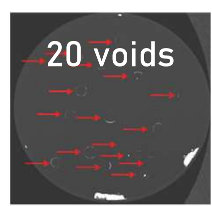

High-density micro mirrors



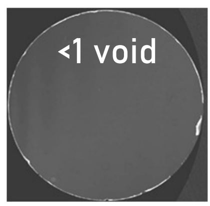
SURFACE ACTIVATION/CLEANING FOR WAFER BONDING

High O* exposure without ions, UV or high temp

Without plasma treatment

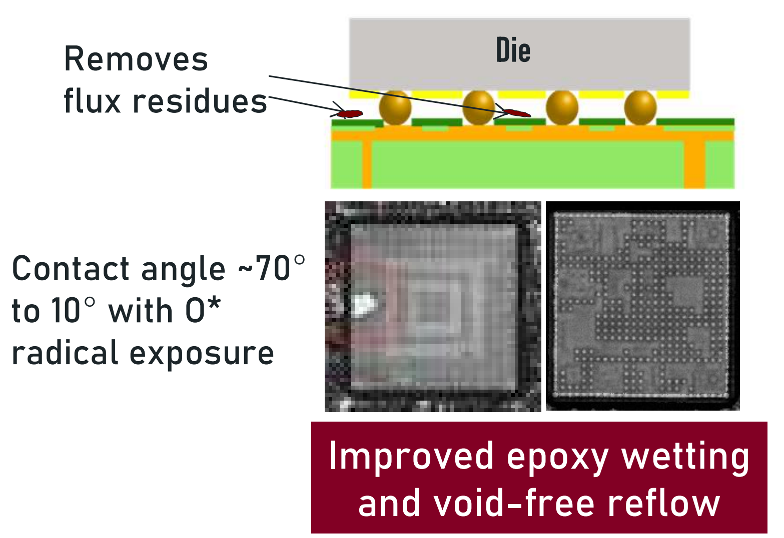


With plasma treatment



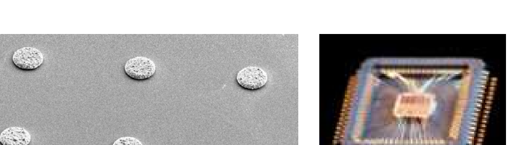
Silicon-to-Silicon
Silicon-to-Quartz

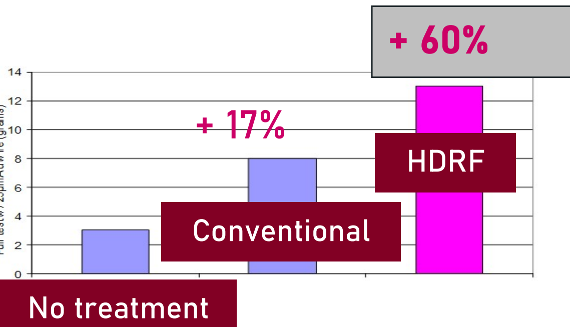
Improved underfill distribution



Reduced ion-impact allows longer radicals exposure.
Lower surface activation energy promotes bonding

Wire Bonding Pad Cleaning





Contamination and/or oxidation removal

TSV Isolation and Seed Layer

F.A.S.T.® CROSSROADS OF ALD AND CVD

(PE)CVD

- CVD mechanisms/precursors
- CCP design
- Hot or cold wall
- 1x channel showerhead

(PE)ALD Monolayer growth

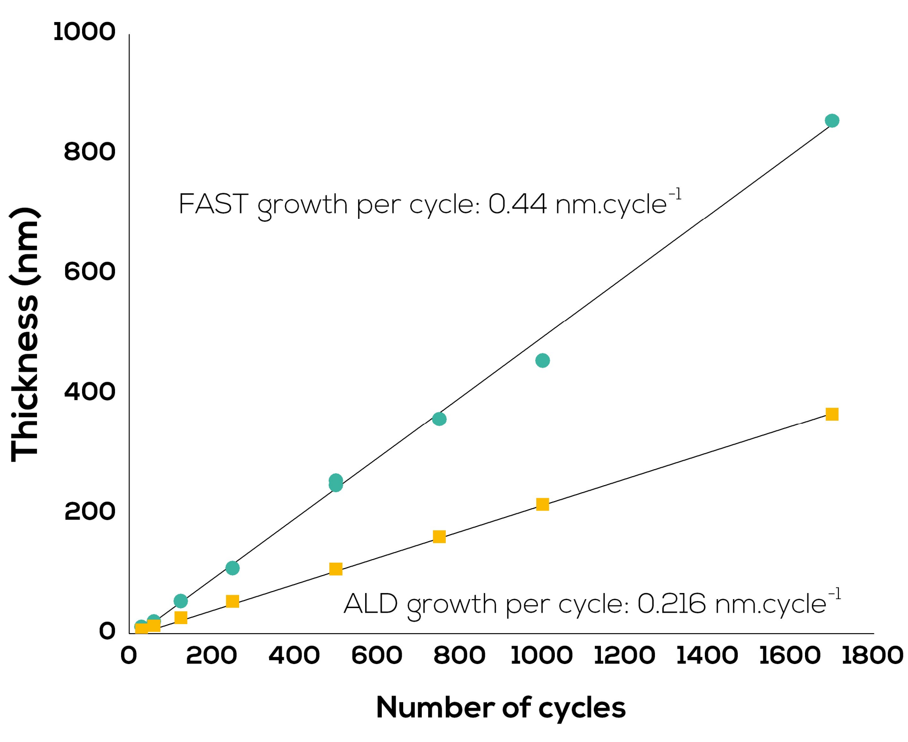
- ALD mechanisms/precursors
- Remote plasma design
- Hot or cold wall
- 1x or 2x channel showerhead

Fast Atomic Sequential Technology

Multilayer growth

- CVD mechanisms/precursors
- CCP design
- Cold wall
- 1x or 2x channel showerhead

F.A.S.T. – AT THE CROSSROADS OF ALD AND CVD



- ALD: Atomic Layer Deposition → one mono-layer per cycle
- FAST: deposition thickness → multiple layer per cycle but faster cycles

LINER TECHNOLOGY APPROACHES FOR TSV

% Conformality

100%
75%
50%
25%
0%

0 5 10 15 20 25 30

Aspect Ratio

ALD

Combined mode
(FAST + ALD)

FAST mode

PECVD

PVD

ALD
PEALD

1nm 1nm 1nm 2nm 2nm 2nm 20nm 20nm 20nm

Process time

Very Thin
&
Conformal

FAST

50nm 40nm 100nm 60nm 1µm 600nm

Process time

Thick
&
Conformal

PECVD

400nm 20nm 800nm 60nm 8µm 100nm

Process time

Very thick
&
Non-
conformal

WIDE MATERIAL RANGE AND APPLICATIONS

Hardmask

Insulators

OXIDES

SiO_2 HfO_2 TiO_2 ZnO Al_2O_3 Ta_2O_5

Metal alloys

METALS

GeSbTe Cu Co W

Conductive films

Plug contact

NITRIDES

TiAlN TiN TaCN TaN SiNx

Protective coatings

TSV Via Etch

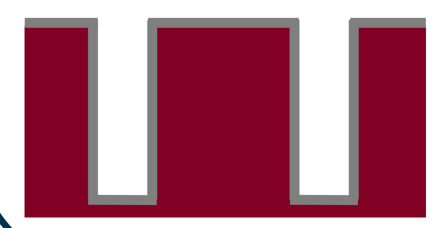
- 10:1 Aspect Ratio
- Smooth sidewalls
- Uniform depth
- Vertical profile
- No undercut

Si DRIE

TSV Insulator

- Continuous
- Conformal
- Leakage/breakdown
- Breakdown
- Adhesion
- Thermal budget

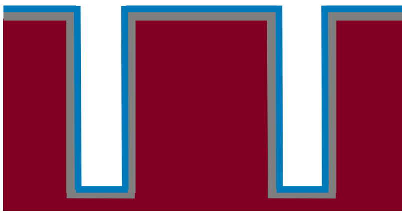
F.A.S.T. SiO_2



TSV Barrier

- Continuous
- Conformal
- Thermal budget
- Copper compatible
- Low resistivity

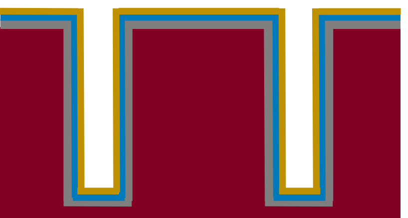
TiN, Co



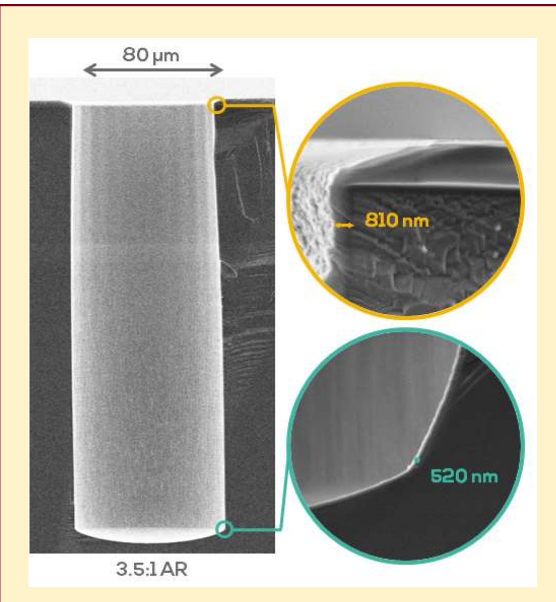
TSV Conductors

- Continuous
- Conformal
- Thermal budget
- Copper compatible
- Low resistivity

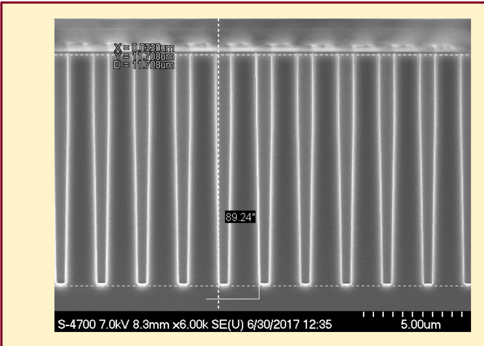
TiN, Cu

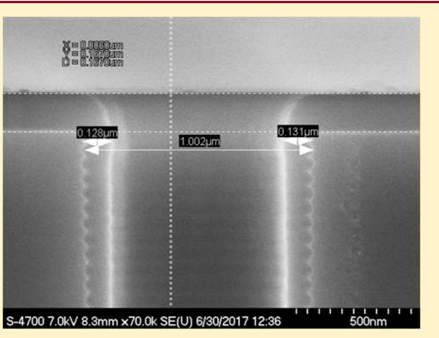


F.A.S.T.® SiO2 LINER COMFORMALITY TUNING (150°C)



- 80 µm x 280 µm, AR 3.5:1
- 100 nm/min @ 150°C
- Conformality: >65%

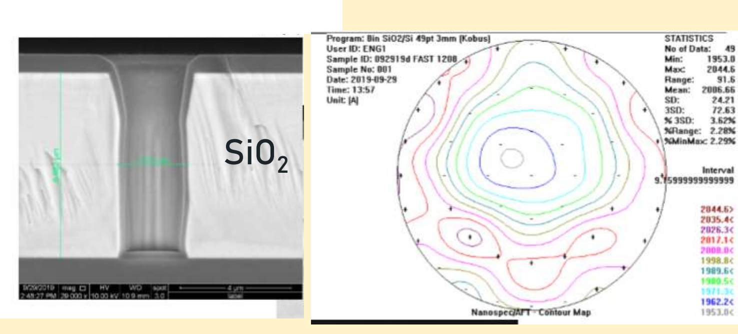




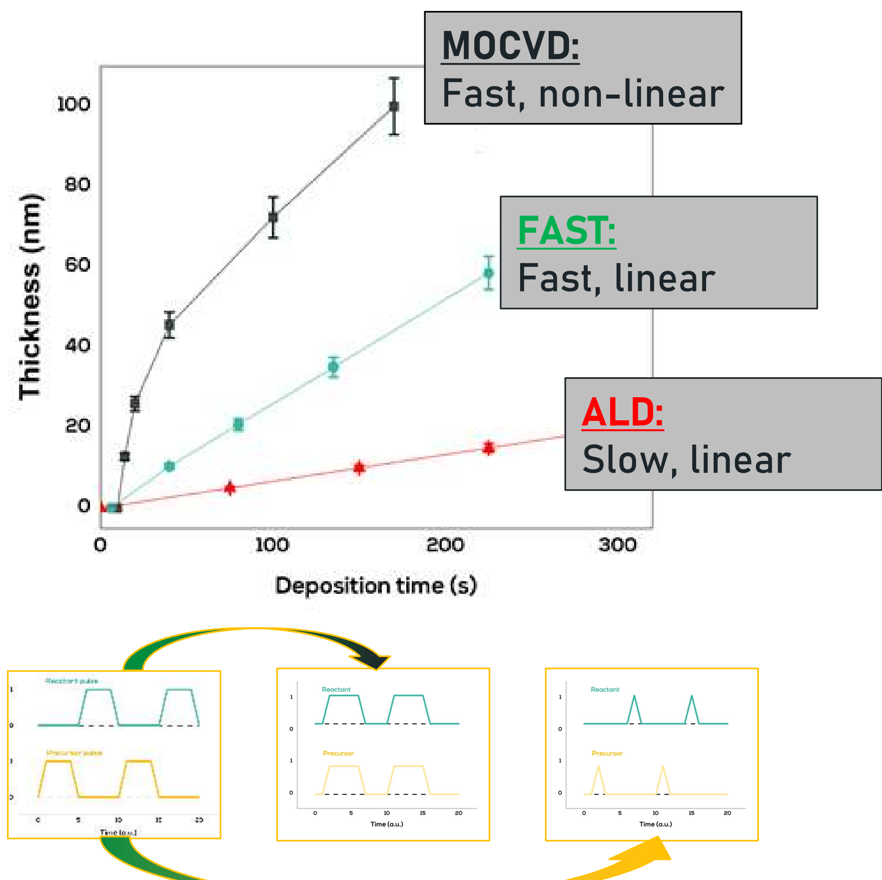
- 1 µm x 12 µm deep, Aspect Ratio: 12:1
- Conformality: 150 nm SiO2 with 50% sidewall coverage

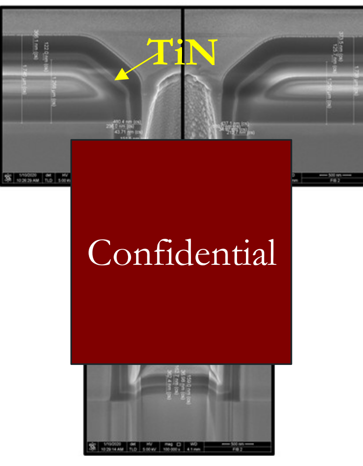
Parameter	Results
Deposition Rate	~ 70 nm/min
Deposition Non-uniformity	< 3%

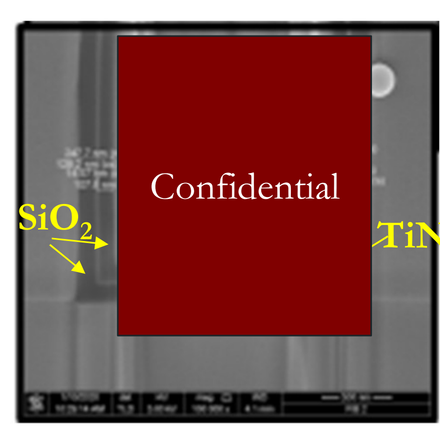
Measurement	Results
Step Coverage (Top/Bottom)	80%
Conformality (Mid-sidewall to bottom)	84%
Conformality (Top to bottom sidewall)	74%



F.A.S.T. - TiN BARRIER TYPICAL PERFORMANCE







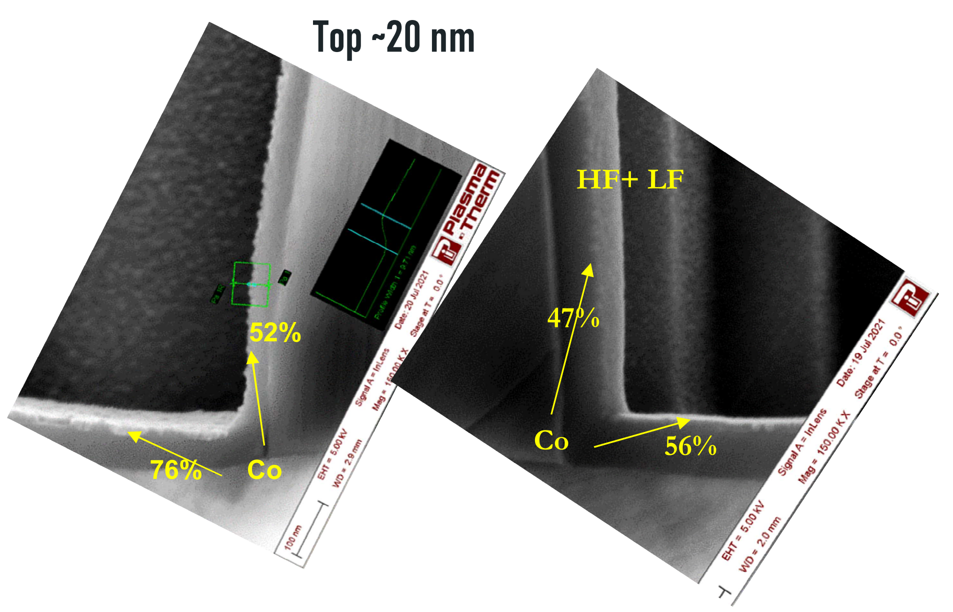
- SiO_2 / TiN / SiO_2 for contrast enhancement
- Pt coating for FIB

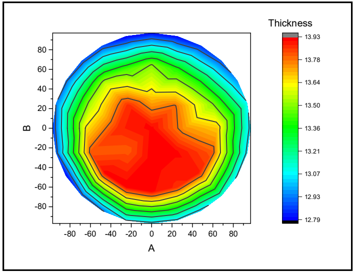
- Precursor: TDEAT
- Temperature: 250°C
- Rate: ~3 nm/min
- Resistivity: 250 to 350 µΩ-cm
- Conformality: ~40 – 50% mid-feature
- Within wafer: ≤±3% (1σ @ 5 mm EE)
- Wafer-to-wafer: ≤±3% (1σ)
- Cleaning: $CF_4/O_2/Ar$

F.A.S.T. Co As BARRIER AND ADHESION LAYER

- FAST @ 250°C
- Vias aspect ratio 4:1
- Precursor: “CoCO” Dicobalt octacarbonyl

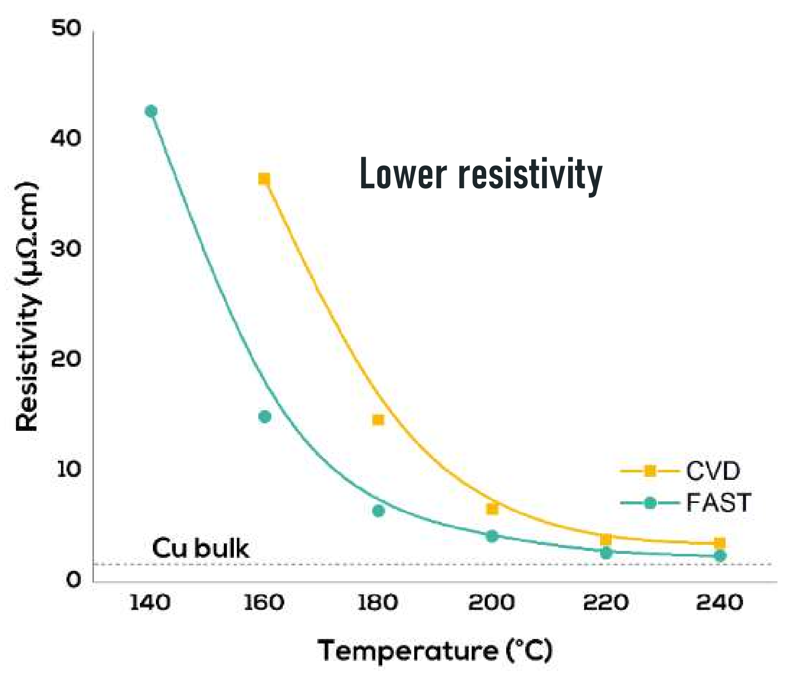
- Characteristics:
  - Deposition rate ~2 nm/min
  - Resistivity <100 µΩ-
  - Conformality >50%
  - Cleans with SF_6



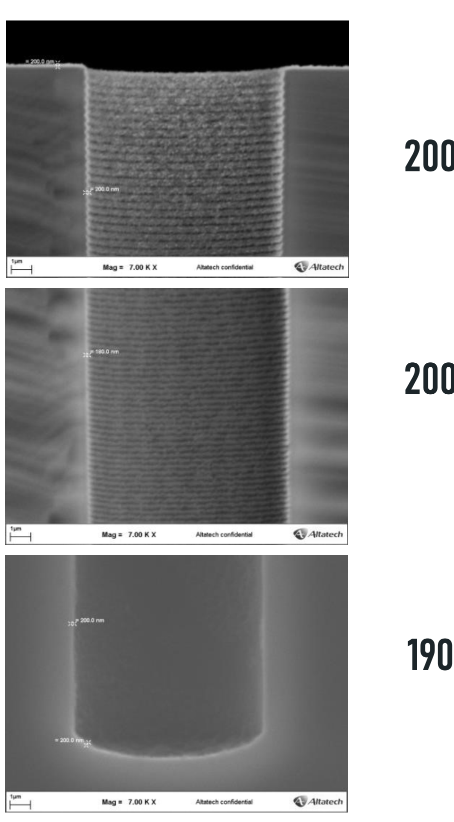


CONDUCTOR EXAMPLE – Cu FILM PERFORMANCES

- Using CupraSelect® precursor and H_2
- Deposition rate >30 nm/min
- Deposition temperature <200°C

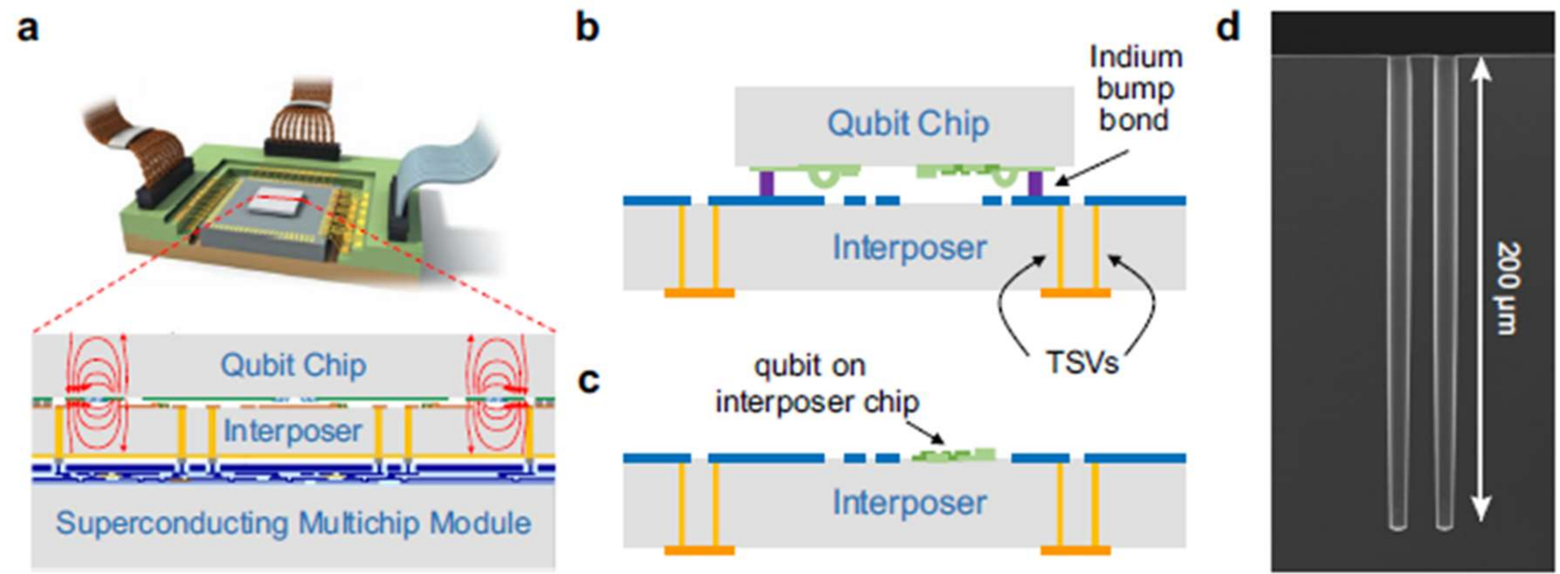


~95% Conformity
10:1 AR

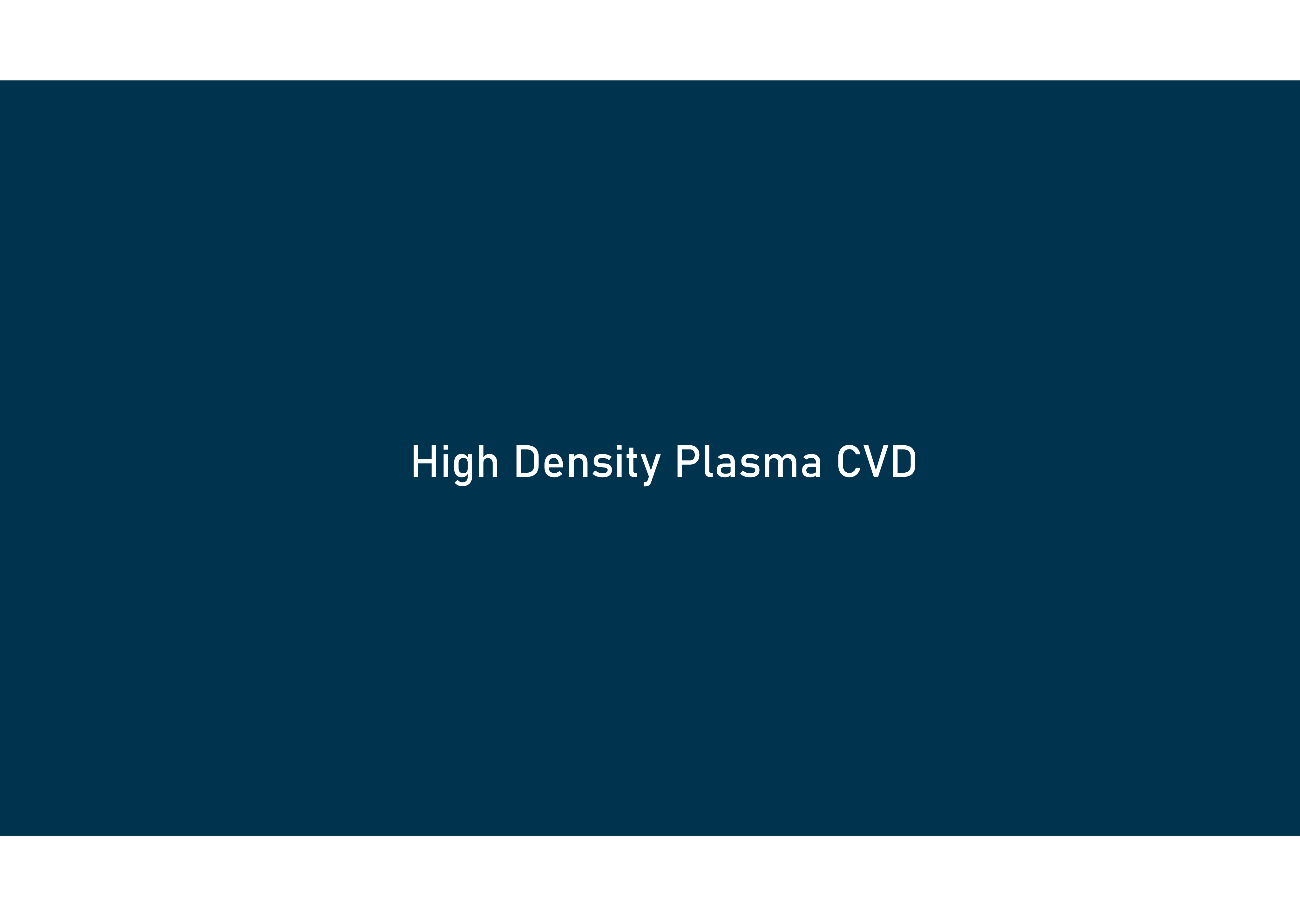


TiN Connector between Qubit and Superconducting Multichip Module

Taking advantage of TiN superconducting properties

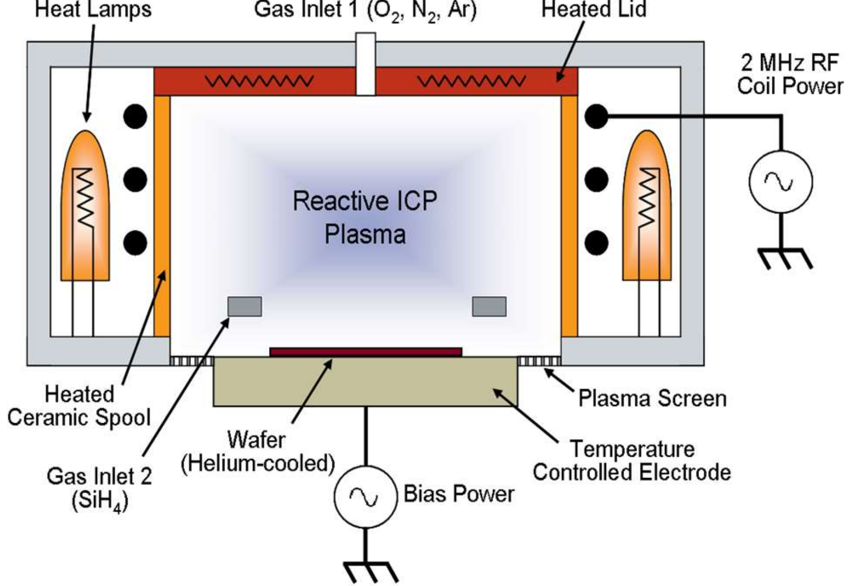


npj Quantum Information (2020) 6:59 ; https://doi.org/10.1038/s41534-020-00289-8,
Solid-state qubits integrated with superconducting through-silicon vias, D. R. W. Yost et. al.


High Density Plasma CVD

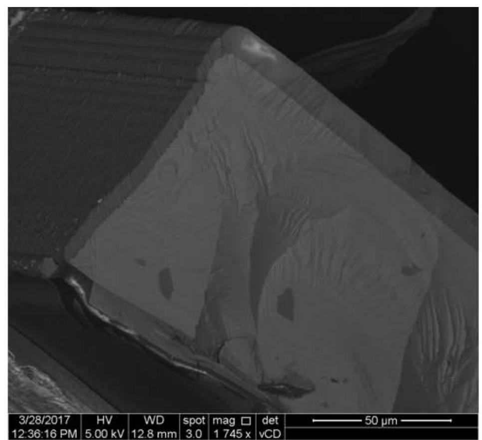
- ICP high density plasma (vs. PECVD)
- Separate gas flows silane precursor and reactants
- Biased substrate
- Clamped substrate
- Lower pressure regime than PECVD

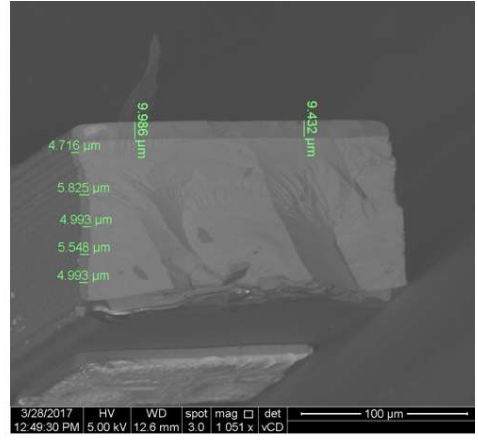
- Applications / Benefits
  - Lower temp operation regime than PECVD
  - Feature fill using bias
  - Lower H content using N_2 instead of NH_3

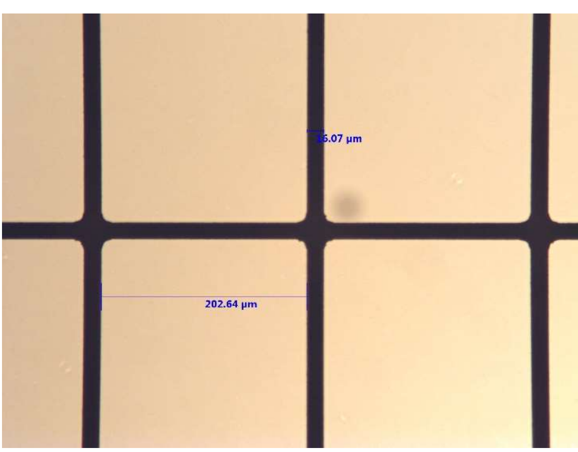


SiNx HDPCVD (60°C) – ENCAPSULATION

- Refractive index ~2.0
- Deposition rate ≥ 1100 A/min
- 50% sidewall coverage at ~6:1 aspect ratio (16 um streets,100 um thick wafer)

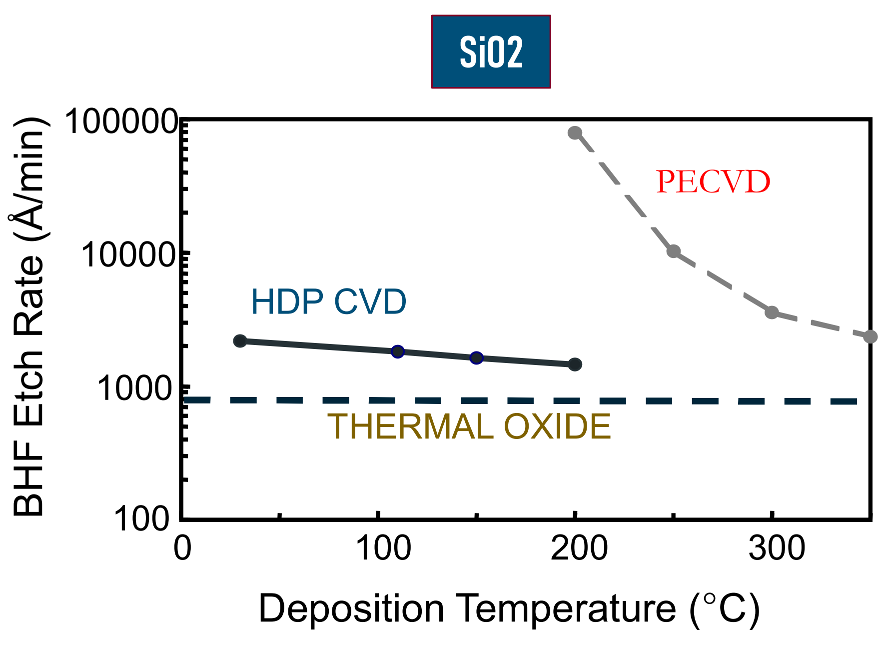




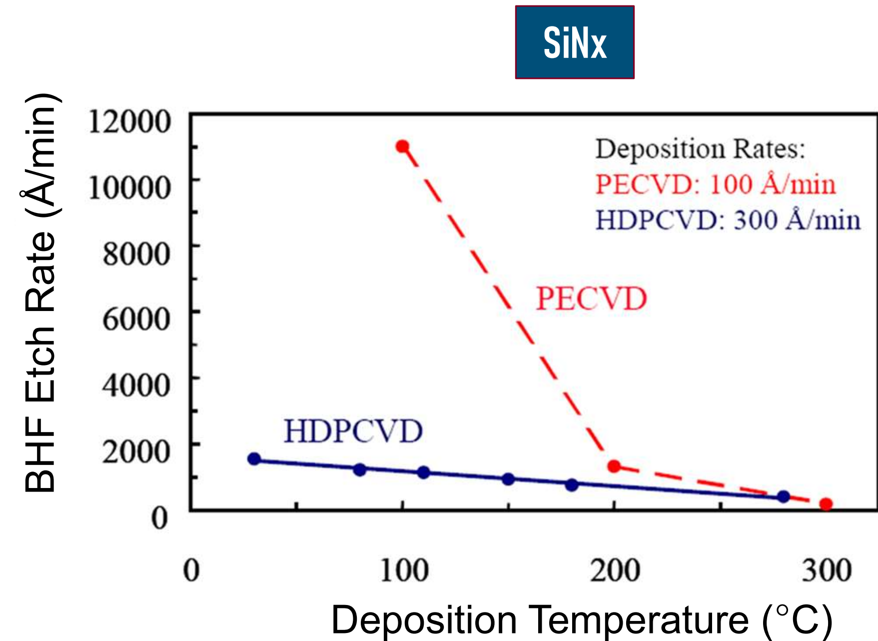


WET ETCH RATE COMPARISON: HDPCVD AND PECVD

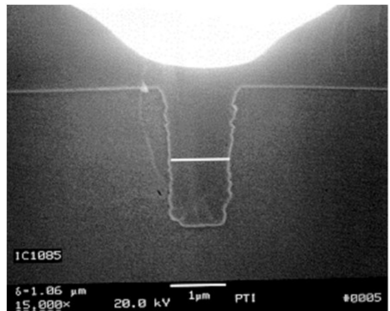
SiO2



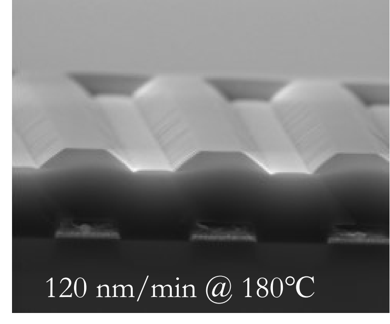
SiNx



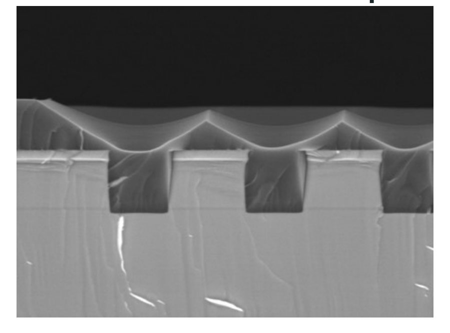
Isolated trench fill

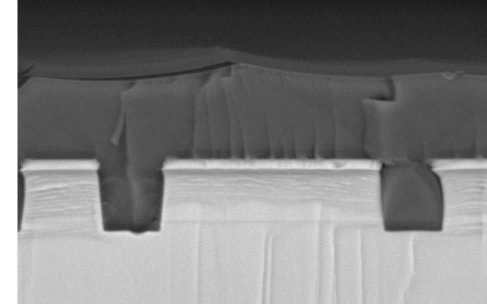


1 µm gap completely filled
AR ~ 2.5:1

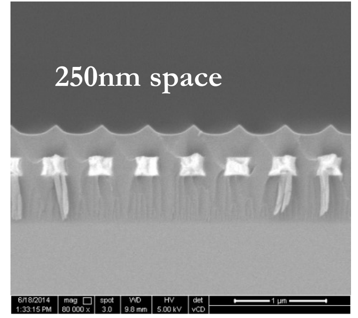


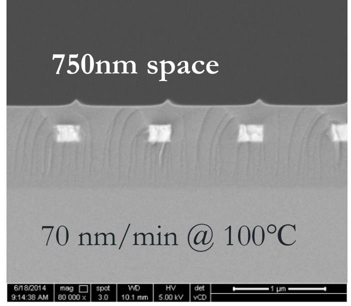
Multiple trench fill

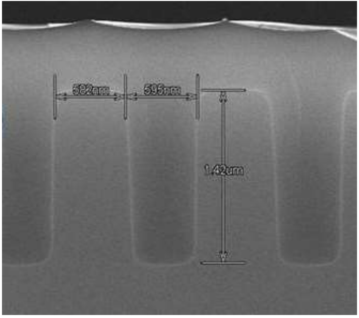




Gap completely filled
and surface nearly planarized

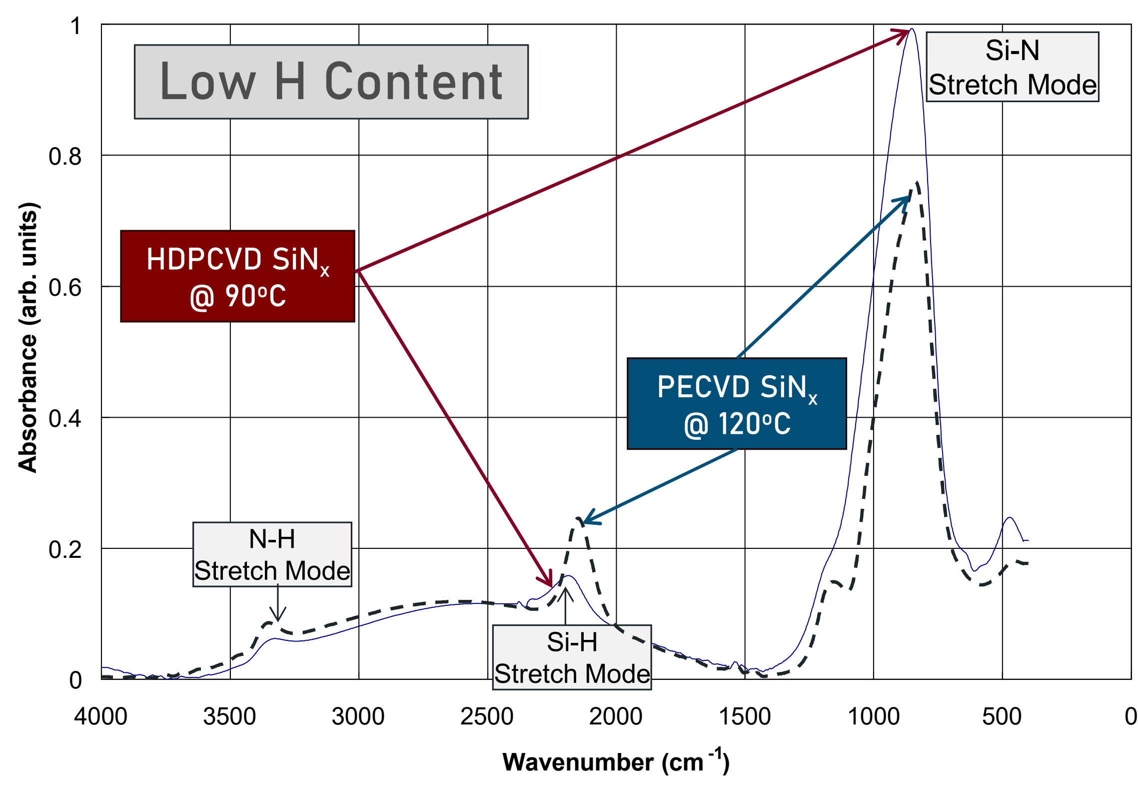


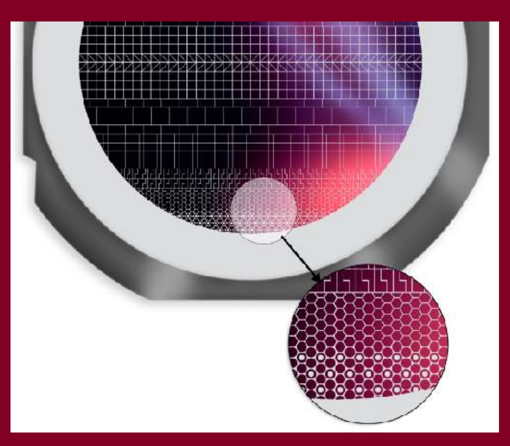




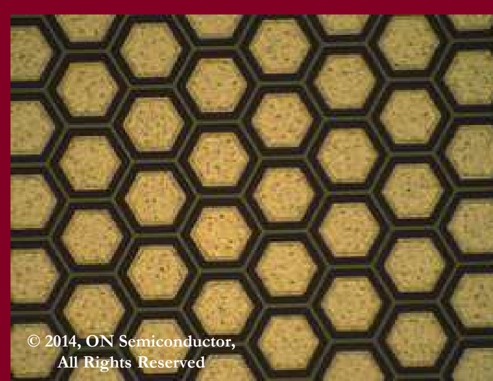
H-CONTENT COMPARISON USING FTIR

SiNx HDPCVD @ 90°C vs. PECVD @ 120°C



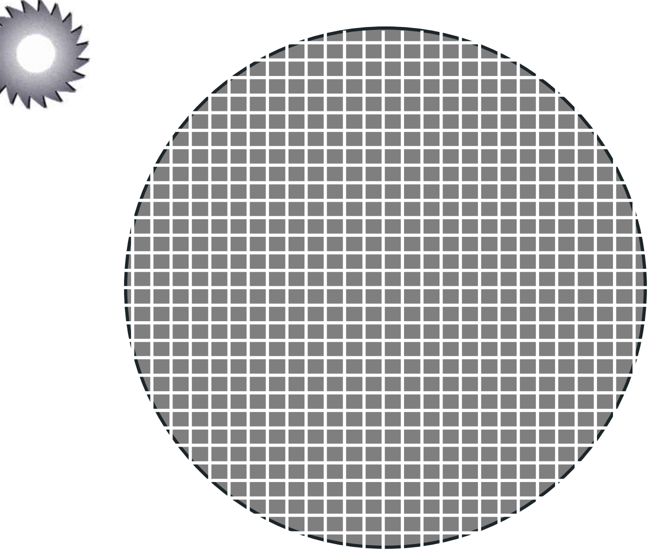


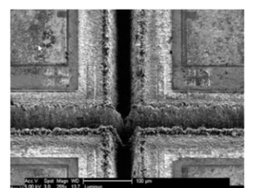
Plasma Dicing

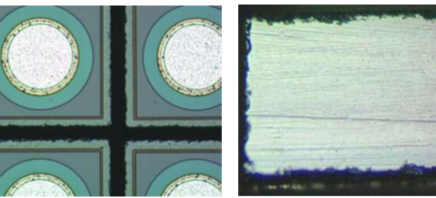


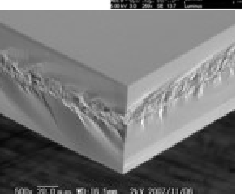
LASER AND SAW DICING METHODS – SEQUENTIAL PROCESSES

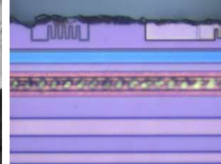
- Wide streets – blade + seal ring
- Damage: Cracks, chips, heat, delamination
- Orthogonal layouts
- Slow for small die
- Slower for thin wafers
- Requires alignment
- Debris, recast and water residues
- Multiple passes for thicker wafers/ multi-material











- Emerging technology using DRIE to simultaneously dice entire wafer
- “Finished“ wafer requires a gentle, low temperature, highly-selective etching solution
- Eliminates most traditional dicing constraints

Wafer Surface – Metals, Dielectrics

Media w/ Exposed Metal

10’s to 100’s of micros of silicon to etch

Plasma

Tape frame

Temperature Sensitive

Tape

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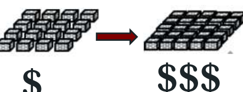
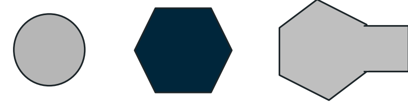
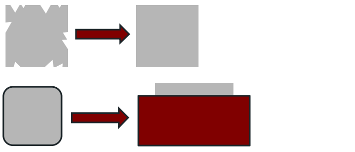
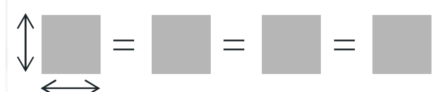
Lower Cost Per Die	▪ Thinner wafers = faster dicing speed 100µm thick wafer < 5 min for dicing
More Die per Wafer	▪ Ultra narrow streets (~ < 5µm) ▪ Less wafer starts, more capacity
No Layout Design Constraints	▪ Freedom to dice any shape, multi-product wafers ▪ Rethink/relocate test/alignment areas
Higher Die Strength & Reliability	▪ No chipping or micro-cracking ▪ No mechanical or thermal stress
Highest Accuracy	▪ Die size variation determined by the mask

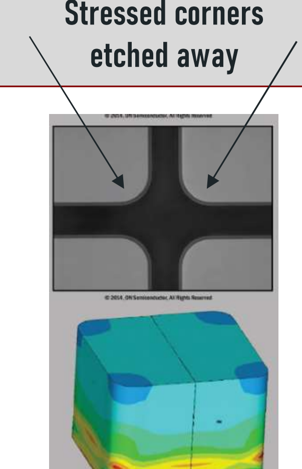




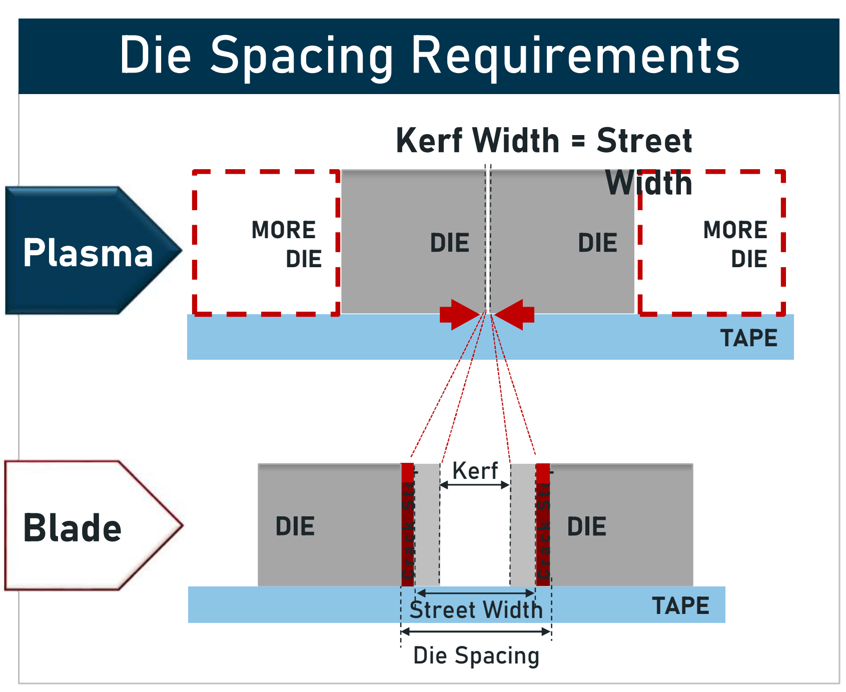




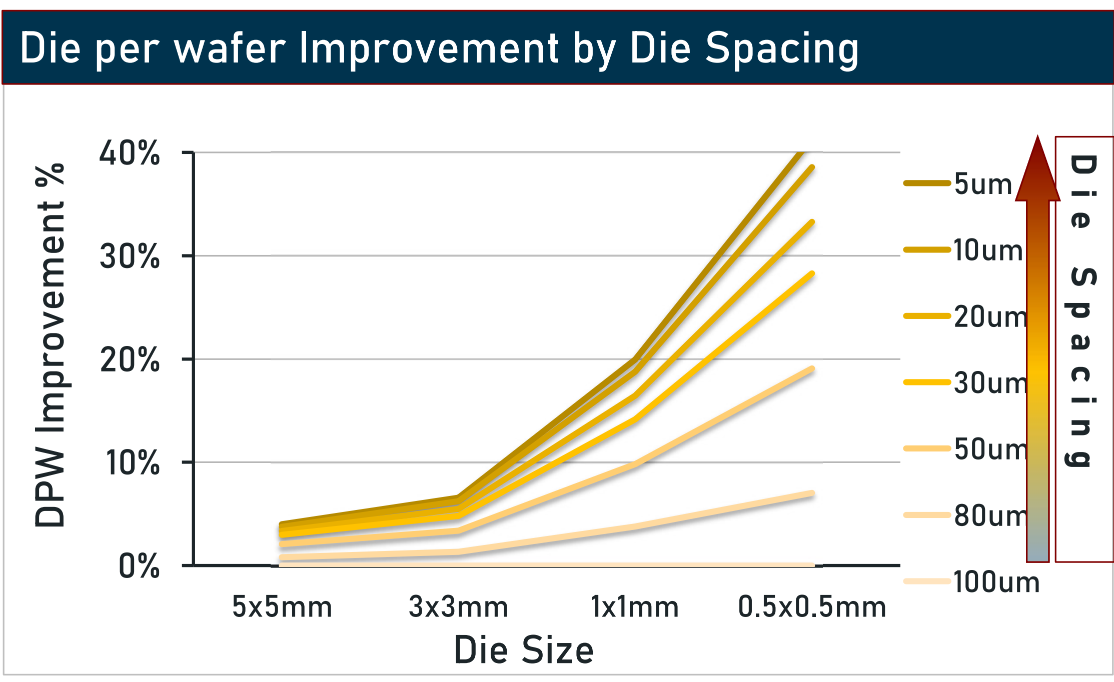
Better reliability
Stressed corners etched away



Die Spacing Requirements

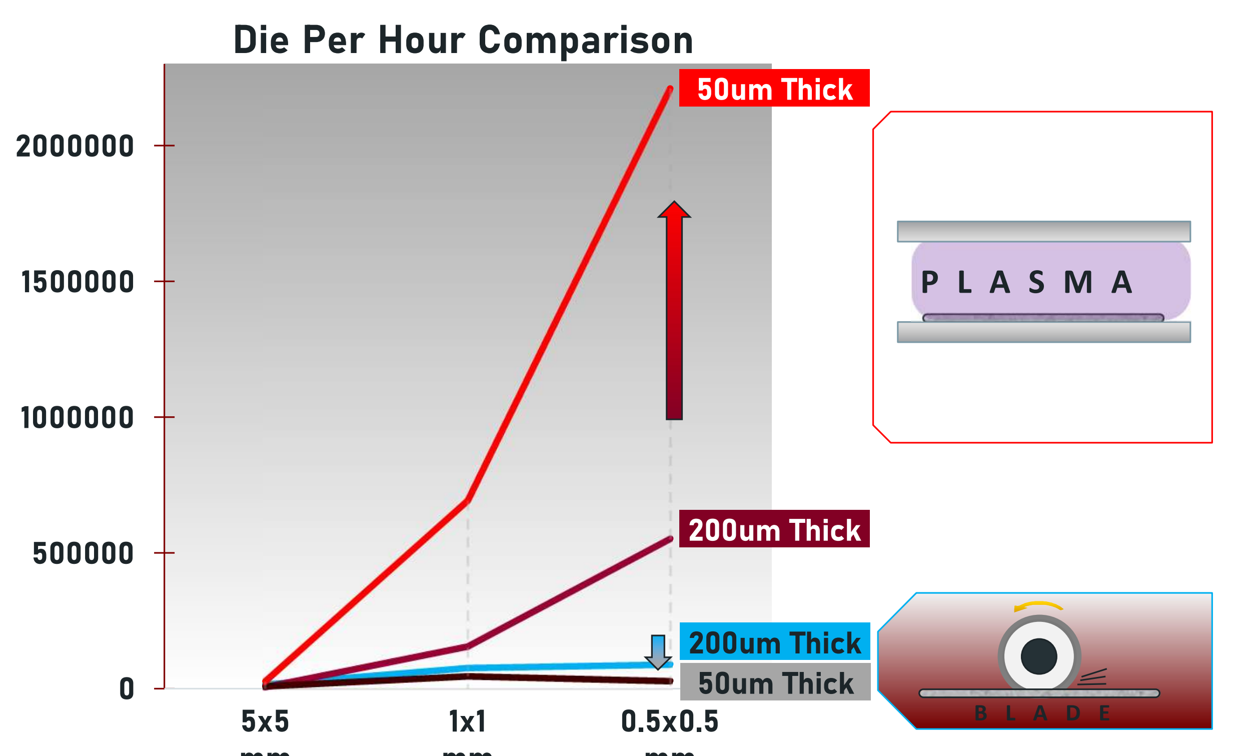


Die per wafer Improvement by Die Spacing



Plasma dicing enables very narrow die spacing, maximizing the die per wafer.

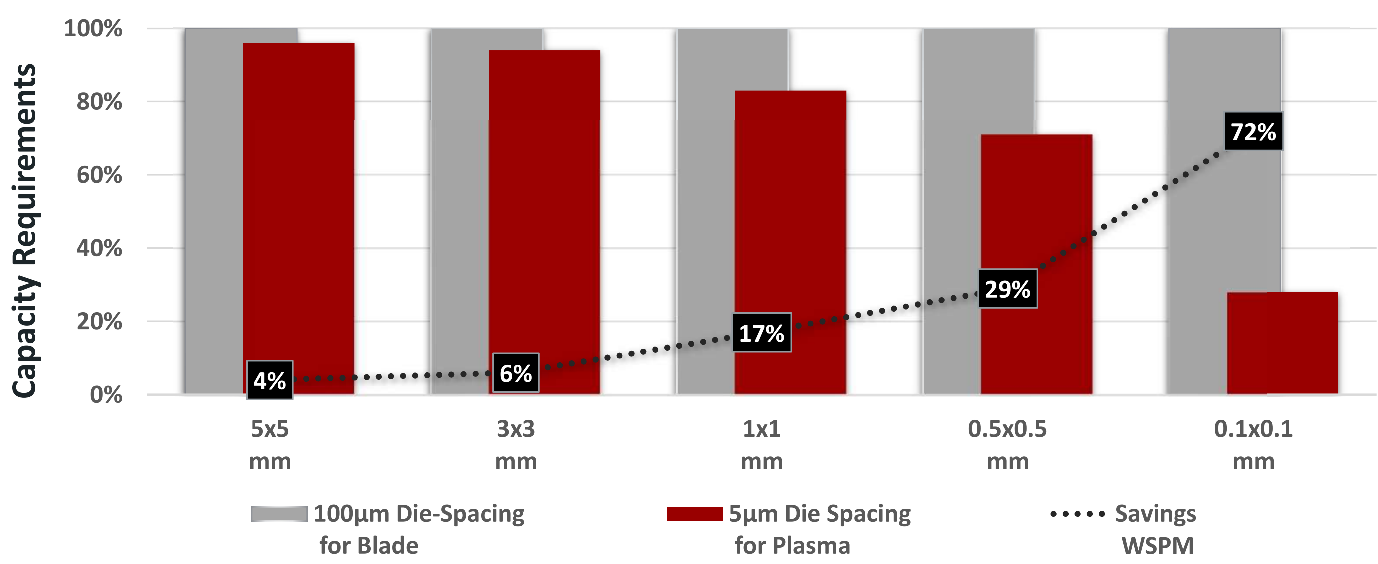
Yield improvements are very significant for most die sizes



Plasma Dicing: Thinner wafers and smaller die **increases** productivity

Saws: Thinner wafers and smaller die **decreases** productivity

- Higher (die per hour) throughputs and higher die per wafer yields → significant economical impact

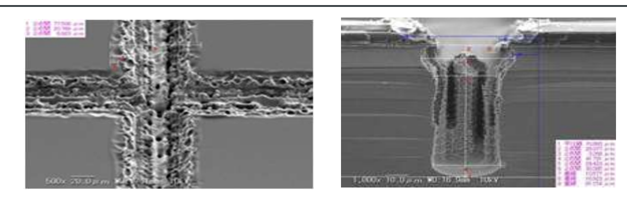


- Fewer wafer starts frees up capacity translating to more product produced, reduced factory space, labor, facilities, utilities and reduced carbon footprint.

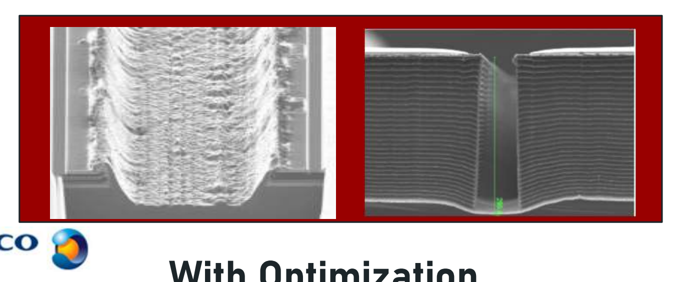
Challenge: Dielectrics and metals on the frontside and backside

Metal layer via Laser Grooving (LG) provides effective, flexible and compatible solution for plasma dicing integration

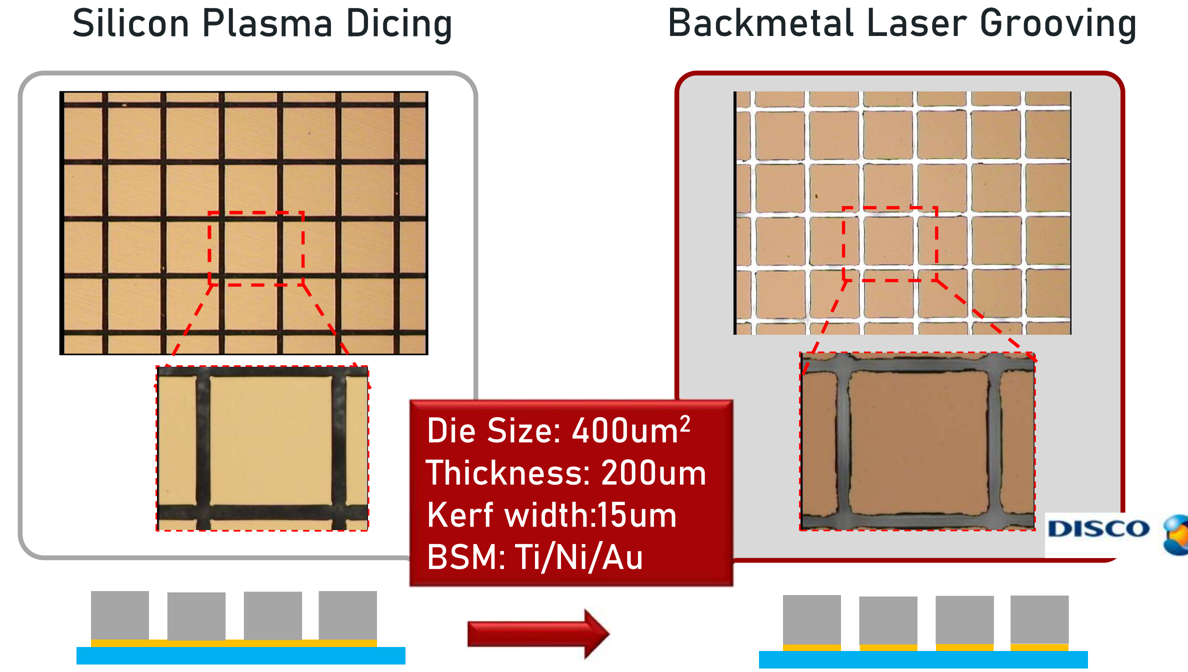
Laser Grooving Evolving for Plasma Dicing Integration



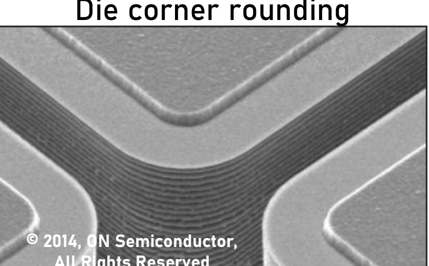
Without Optimization



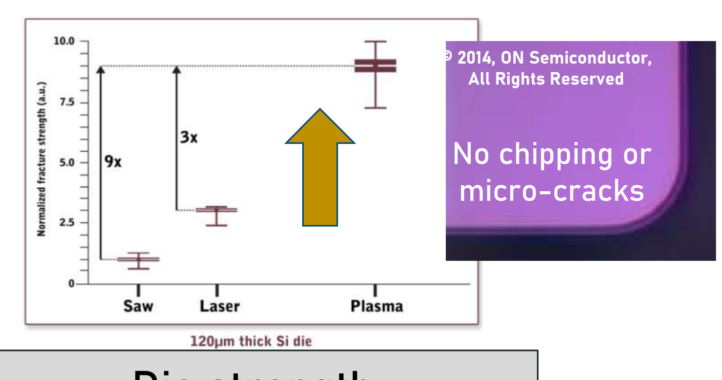
With Optimization



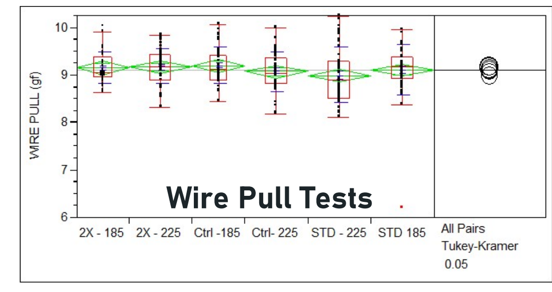
Die corner rounding



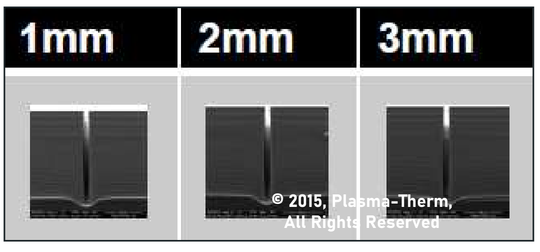
Die attach stress



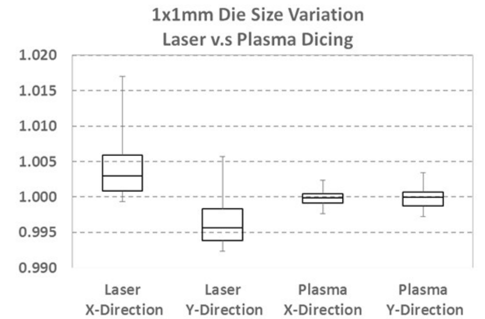
Die strength



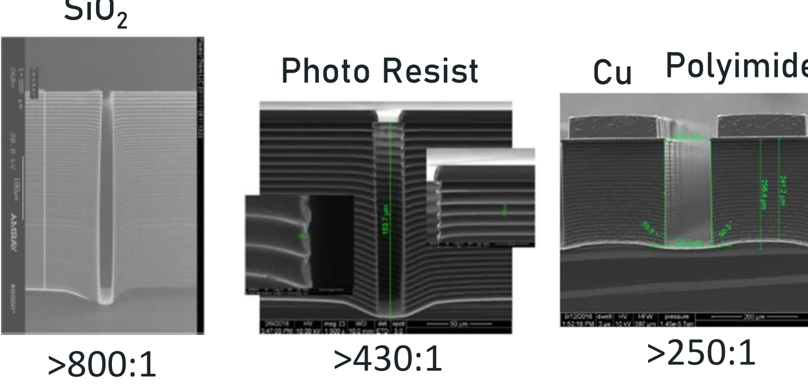
Bond pad strength



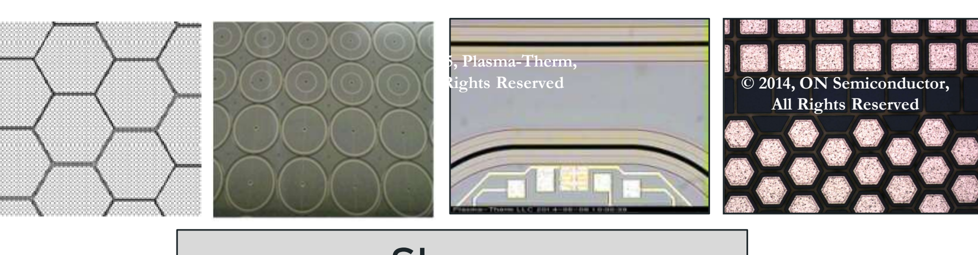
Tilt/skew



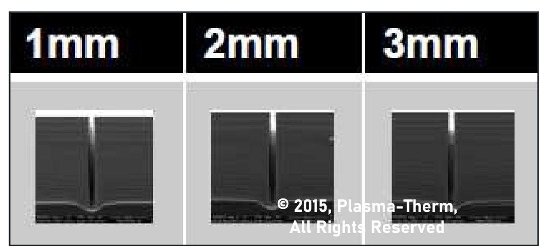
Die dimension accuracy



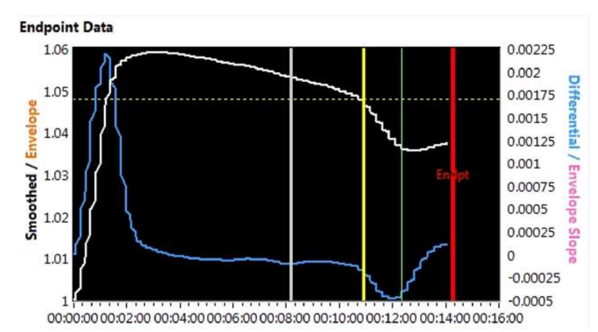
Mask materials



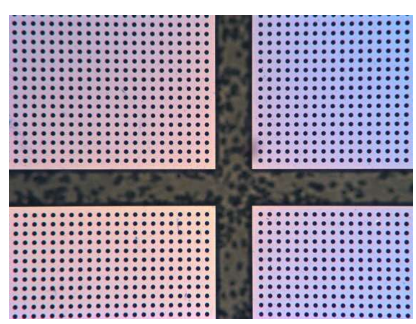
Shapes



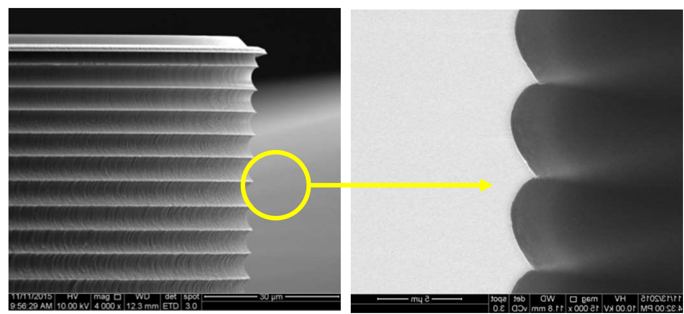
Tilt / Skew Control



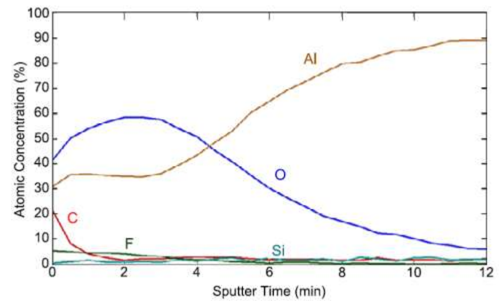
Endpoint control (<1% Exp. Si)



Dicing + Thru wafer holes
(same process recipe – Endpoint control)



Polymer free process



Contamination Control

	Qualified Applications						
	Power	**LED**	**RFID**	**IR Image sensor**	**3D MEMS**	**III-V**	**CMOS**
Wafer size	6 & 8”	4 & 6”	8”	8”	8”	3 & 4”	8” & 12”
Wafer type	Si, GaN/Si	Si, Ge	Si	Si	Si	GaAs	Si
Street size	10-15um	<5µm	7µm	Round die	20µm	20µm	10-50um
Wafer thickness	50-250um	120µm	100µm	760µm	100+300µm	50-300um	50-775um
Assembly	Wirebond Flip Chip	Wirebond	Flip Chip	Confidential	Flip Chip	Wirebond	Flip Chip
	© 2014, ON Semiconductor, All Rights Reserved	Confidential	7µm street	© 2014 Plasma Therm All Rights Reserved	Confidential	Confidential	

Thank you for your contributions and materials to prepare this presentation

Christopher Johnston, Plasma-Therm
Thierry Lazerand, Plasma-Therm
Dr. Marco Notarianni, Plasma-Therm
Dr. Kenneth Mackenzie, Plasma-Therm
Yannick Pilloux, Plasma-Therm
Dr. Julien Vitiello, Plasma-Therm
Gordy Grivna, ON Semiconductor
Jason Doub, ON Semiconductor
Dr. Tomotak Tabushi, DISCO
Dr. Frank Wei, DISCO
Hideyuki Sando, DISCO
JS Jung, DISCO

Web: www.plasmatherm.com

E-mail: sales@plasmatherm.com