



# Microelectronics/ Semiconductor Research Community Virtual Workshop



September 8 and 9, 2022 12pm – 3:30 pm EDT

Hosted by NSF National Nanofabrication Coordinated Infrastructure (NNCI) Program

Organizers: Philip Wong (Stanford), Trevor Thornton (Arizona State),  
Shyam Aravamudhan (North Carolina A&T Univ.) and Sanjay Banerjee (Univ. of Texas)

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## OVERVIEW:

The NSF NNCI program supports a geographically distributed network of university cleanroom user facilities across the Nation for microelectronics and nanotechnology research. In light of the recent efforts of the federal government to bolster semiconductor manufacturing in the US under the auspices of the CHIPS Act, NSF NNCI is organizing a two-day online workshop to examine how NNCI can interact with the various components of the CHIPS initiative. Tentatively, we envision four sessions consisting of invited talks by leading researchers in academia and industry focused on academic research infrastructure, workforce development, manufacturing and semiconductor R&D. Some of issues and questions we hope to cover are:

- 1) Semiconductor R& D: What are the trends in logic, memory, analog/mixed signal, 6G, power, packaging, and heterogeneous integration?
- 2) Advanced Manufacturing: What are the advances and challenges in materials, equipment, and metrology development in the next decade? What EDA and TCAD tools need to be developed?
- 3) Academic Infrastructure: What sort of equipment and at what wafer sizes should NNCI invest in? How are the equipment and staff going to be sustained? What should be the goals of the academic infrastructure?
- 4) Workforce Development: How do we encourage undergraduates to get interested in semiconductors and nanoelectronics? How do we minimize leakage of the talent pipeline to other industries that use the same skill sets? How do we build up a cadre of technicians in this area using community colleges?

The anticipated outcome of this workshop will be developing a report that could inform CHIPS funding as it relates to USICA, NSTC, NAMP and the Microelectronics Commons, as well as NSF Engines and FuSe.

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## SCHEDULE:

TIME (EDT)	DAY 1 Thursday; September 8, 2022	DAY 2 Friday; September 9, 2022
12:00pm – 1:30pm	<b>SESSION 1</b> <b>R&amp;D Challenges</b> Chair: H.S. Philip Wong (Stanford)	<b>SESSION 3</b> <b>Workforce Development</b> Chair: Shyam Aravamudhan (NC A&T Univ.)
	<b>Invited Speaker Presentations:</b>	<b>Invited Speaker Presentations:</b>
12:00pm	Welcome, Introduction (Sanjay Banerjee)	Welcome, Day 1 Summary (Sanjay Banerjee)
12:15pm	Jack Kavalieros (Intel Fellow)	Tsu-Jae King Liu (Dean of Eng., Berkeley)
12:45pm	Nirmal Ramaswamy (VP, Micron)	Gabriela Cruz Thomas (Director of Univ. Research, Intel)
1:15pm	Vijay Narayan (IBM Fellow)	<b>Panel Discussion:</b> Peter Bermel* (Purdue), Emmanuel Giannelis* (Cornell), Rick McCormick (Sandia)
1:45pm	<b>Break</b>	<b>Break</b>
2pm – 3:30pm	<b>SESSION 2</b> <b>Materials, Supplies, &amp; Equipment</b> Chair: Trevor Thornton (ASU)	<b>SESSION 4</b> <b>Academic Infrastructure</b> Chair: Sanjay Banerjee (U Texas)
	<b>Invited Speaker Presentations:</b>	<b>Invited Speaker Presentations:</b>
2:00pm	Mike Chudzik (VP, AMAT)	Oliver Brand (NNCI)
2:30pm	Victor Moroz (Synopsys Fellow)	Jesus del Alamo (MIT)
3:00pm	Prith Banerjee (Ansys CTO)	<b>Panel Discussion:</b> Raj Jammy* (Mitre), Larry Goldberg (NSF), Jim Plummer (Stanford)

(Precise times subject to change)

Panel Discussion Chairs\*

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DAY 1 SPEAKERS, PANELISTS, AND ORGANIZERS:

SESSION 1 (R&D Challenges)



**H.S. Philip Wong**  
Director of SNF  
Stanford  
**(Session Chair)**



**Jack Kavalieros**  
Intel Fellow  
Intel Corporation



**Vijay Narayanan**  
Fellow, Senior Manager +  
Strategist  
IBM



**Nirmal Ramaswamy**  
VP of Advanced DRAM +  
Emerging Memory  
Micron Technology

SESSION 2 (Materials, Supplies, & Equipment)



**Trevor Thornton**  
Professor of Electrical,  
Computer, & Energy  
Engineering  
Arizona State University  
**(Session Chair)**



**Michael Chudzik**  
VP of Process Development,  
Device Integration, &  
Program Management  
Applied Materials



**Victor Moroz**  
Synopsys Fellow  
Custom Design Manu. Group  
Synopsys



**Prith Banerjee**  
Chief Technology Officer  
ANSYS Inc

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DAY 2 SPEAKERS, PANELISTS, AND ORGANIZERS:

SESSION 3 (Workforce Development)



**Shyam Aravamudhan**  
Director of Core Facilities at  
Joint School of Nanoscience  
& Nanoengineering  
North Carolina A&T State  
University  
**(Session Chair)**



**Tsu-Jae Liu**  
Dean and Roy W. Carlson  
Professor of Engineering  
University of California,  
Berkeley



**Gabriela Cruz Thomas**  
Director of University  
Research and Collaboration  
Intel Corporation



**Peter Bermel**  
Associate Professor  
Purdue University



**Emmanuel Giannelis**  
VP for Research and  
Innovation  
Cornell University



**Rick McCormick**  
Principal Scientist  
Sandia National Labs

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DAY 2 SPEAKERS, PANELISTS, AND ORGANIZERS (CONTINUED):

SESSION 4 (Academic Infrastructure)



**Sanjay Banerjee**  
Director of Microelectronics  
Research Center  
Univ. of Texas, Austin  
(Session Chair)



**Oliver Brand**  
Executive Director at Georgia  
Tech  
and NNCI Director



**Jesús del Alamo**  
Director of Microsystems  
Technology Laboratories  
MIT



**Raj Jammy**  
Chief Technology Officer  
Mitre Engenuity



**Larry Goldberg**  
Senior Advisor  
NSF



**Jim Plummer**  
John M Fluke Professor of  
Electrical Engineering  
Stanford

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