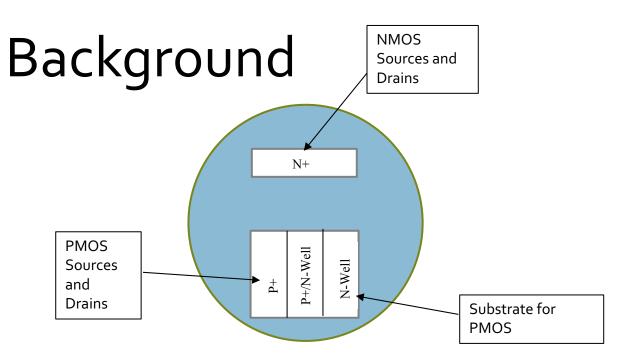
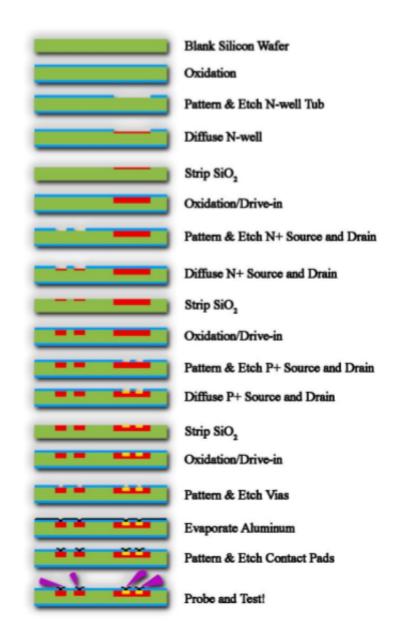
TRANSISTOR PROCESS OPTIMIZATION FOR MICROFABRICATION COURSES

Calvin M. Jones, Tristan Cunderla

Advisors: Dr. David Dickensheets, Dr. Todd Kaiser, Dr. Phil Himmer,

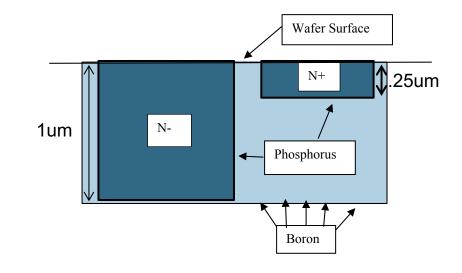


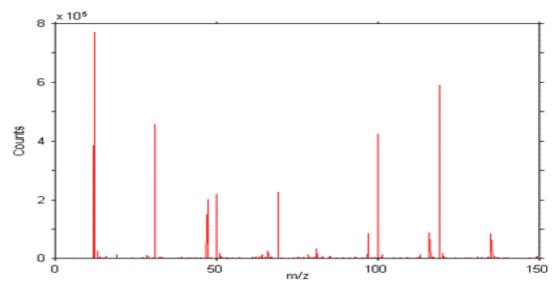
- Micro-Fabrication courses based on diffusion process
- Wafers consist of N-, N+, P+, and P+N- regions
- Wafer doped with phosphorus in N- and N+ and boron in P+
- Doping concentration and dopant profiles important variables in limiting transistor functionality
- Failures with NMOS and PMOS with major failure occurring in PMOS



Background

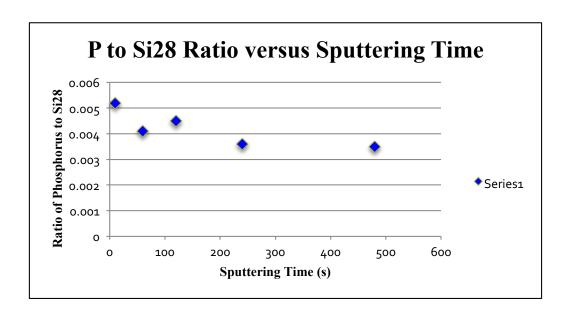
- Ideal depth profile
- Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) used for phosphorus search
- Sputter and create spectra

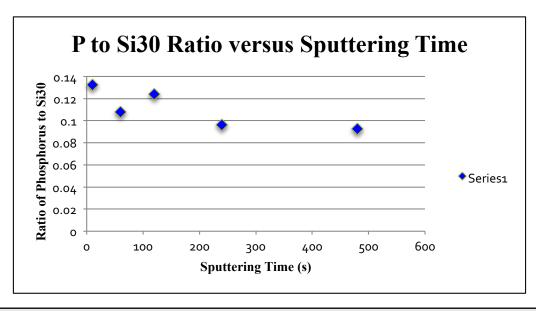




Initial Testing

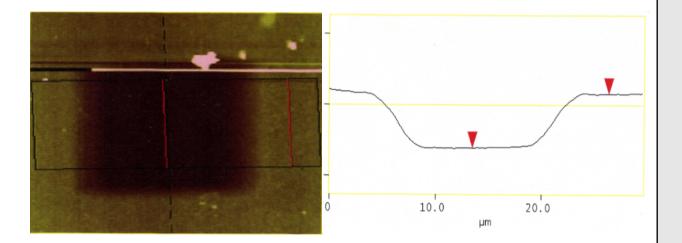
 Phosphorus to silicon ratio in relation to sputtering time using ToF-SIMS

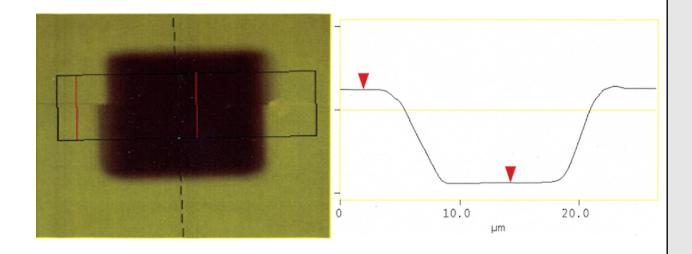




Depth Analysis

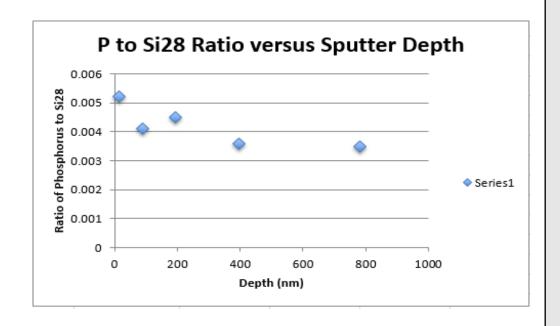
- Sputter locations tracked by sputter times
- Atomic Force Microscope (AFM) used to find depths

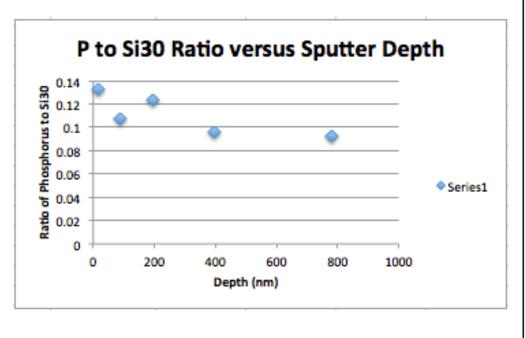




Depth Analysis

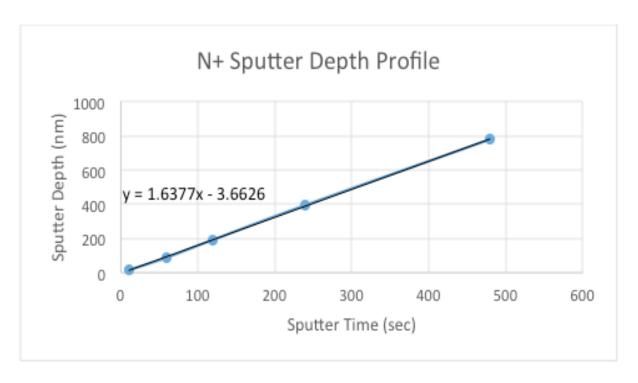
- AFM data was used to relate sputtering time to depth
- Phosphorus to Silicon Ratio was then compared to depths
- Phosphorus found at significantly deeper levels than expected in N+ region





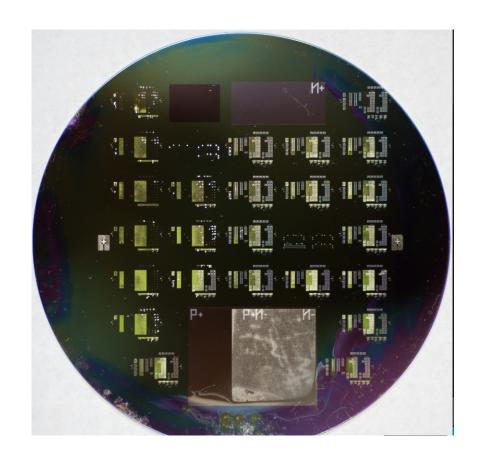
Depth Profile

- Depth profile created using the found relationship between sputtering time and depth.
- Blank phosphorus doped wafers used to confirm profile
- Research analysis based on depth profile



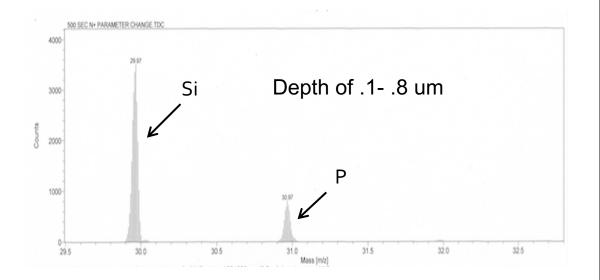
Parameter Changes

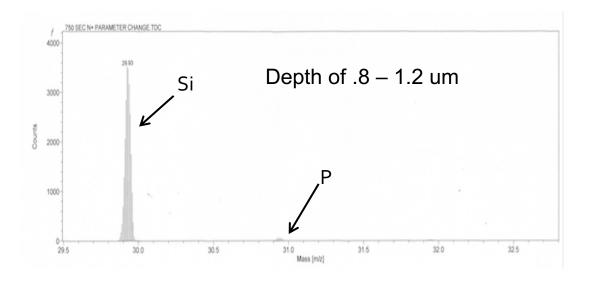
- Based on the found depth profile new wafers were made with changed parameters
- Temperature decrease of 25°C for N-well diffusion
- Temperature increase of 50°C for N-well diffusion
- Temperature decrease of 50°C for N+ diffusion
- Control Wafers were also made for comparison



Results

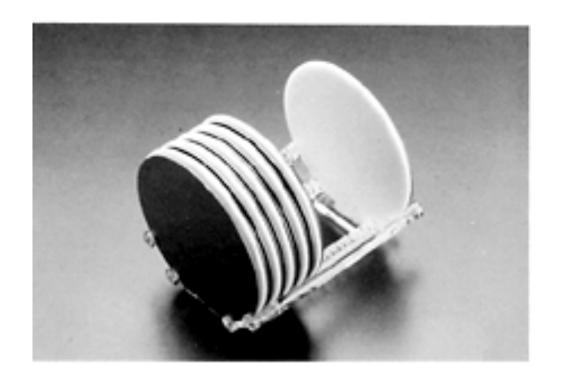
- New wafers were tested with ToF-SIMS using new depth profile
- N+ region with changed parameter observed
- Sputter performed for 30, 500 and 750 seconds
- Phosphorus removed between 500 and 750 seconds or .8-1.2 um





Conclusion

- The depth profile for the wafers shows that phosphorus is much deeper than expected
- Reduction of the phosphorus depth after the parameter change suggests the issue is related to the diffusion sources
- Since minor temperature changes still produced too deep of a depth profile, a greater change in temperature in addition to a change in diffusion time should be tested
- Newly fabricated wafers will continue to be tested



Acknowledgements

- National Nanotechnology Coordinated Infrastructure (NNCI)
- National Science Foundation (NSF)
- Montana Micro-fabrication Facility (MMF)
- Imaging and Chemical Analysis (ICAL)



References

- Richard C. Jaeger, "Diffusion" in *Introduction To Microelectronic Fabrication*, 2nd *Edition* New Jersey, 2002 Prentice Hall
- Matthew Leone, Todd Kaiser, *CMOS Lab Manual*, Bozeman, 2012 Montana State University
- http://www.techneglas.com/products/techprod/techneglas/pages/phos_pg6.htm
- http://www.physics.montana.edu/ical/instrumentation/sims.html