The University of Texas at Austin
Cockrell School of Engineering

Fabrication and Optimization of a Schottky Diode Utilizing Field Plate Termination

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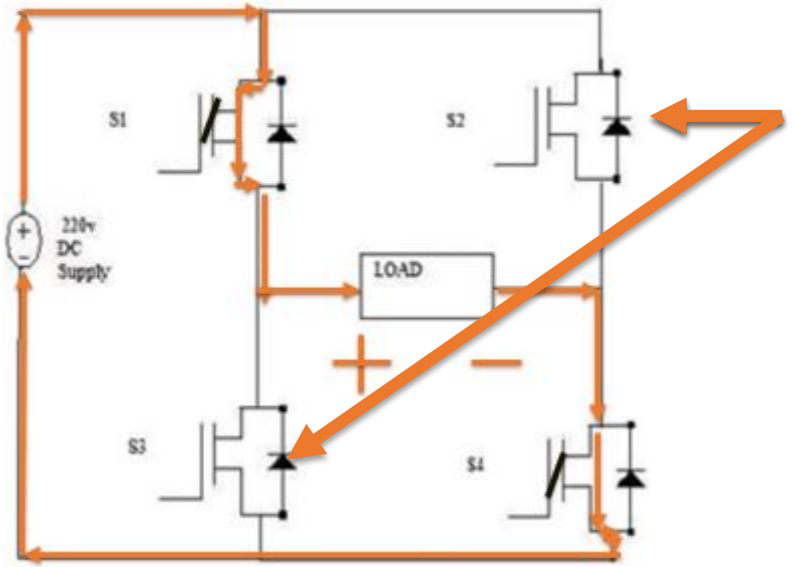
SPEC
Semiconductor Power Electronics Center

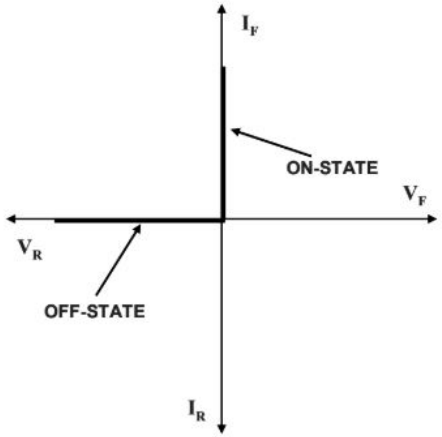
Introduction to Power Devices

- Application: High power conversion systems
- Ideal power devices:
  - Support high current and voltage
  - Block current under one voltage bias (OFF) and conduct in the other (ON)
  - Switch rapidly



OFF
Blocking

H-Bridge inverter



Introduction to Power Devices

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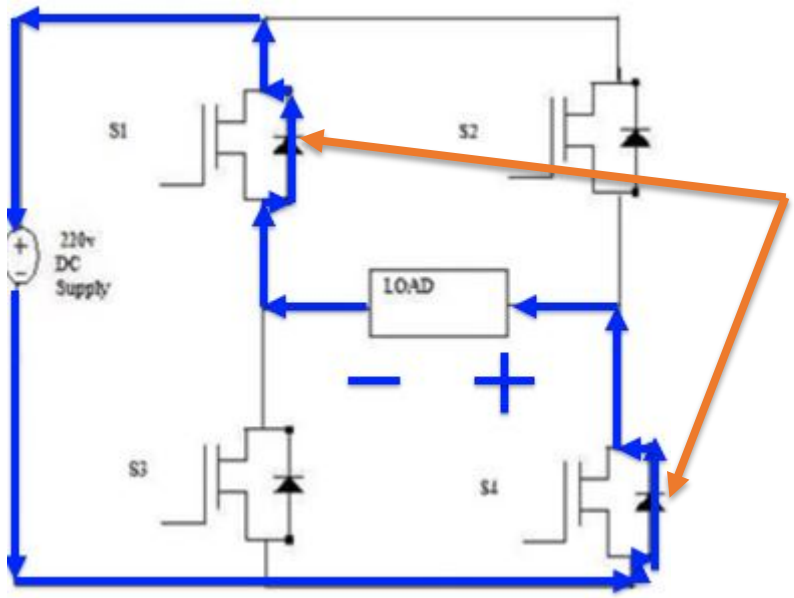


ON
Conducting

H-Bridge inverter

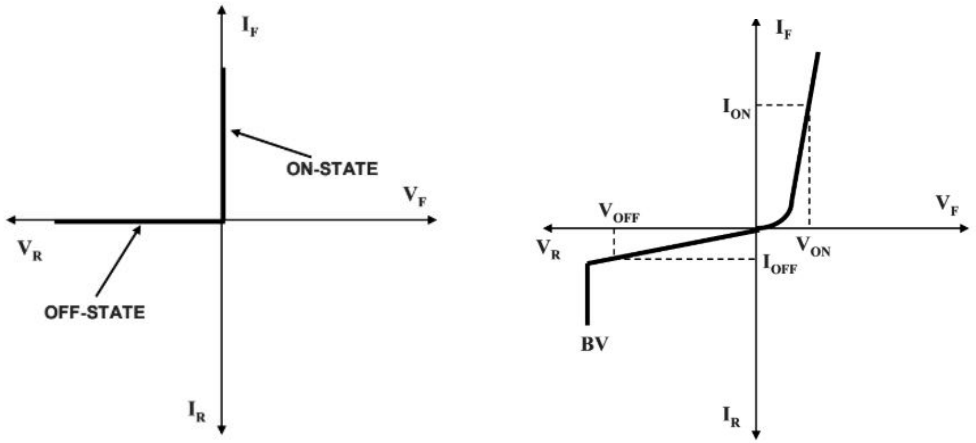


Fig. 1 Power device IV curves
Adapted from *Fundamentals of Power Semiconductor Devices* (6), By B.J. Baliga, 2008, New York City, 2008

Schottky Power Devices

- **Negligible charge build up in ON state- fast switching**

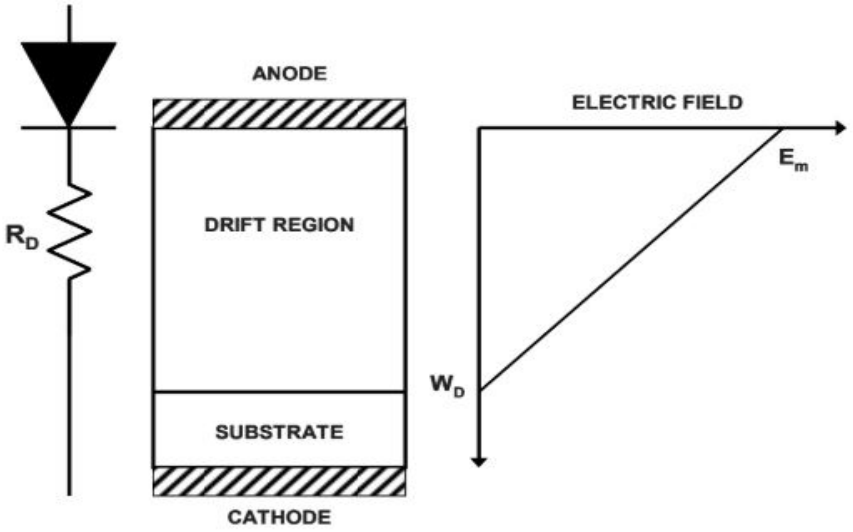
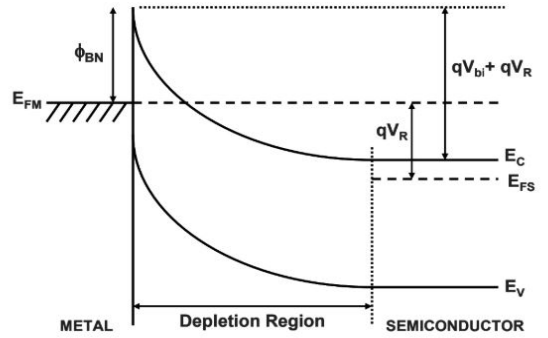
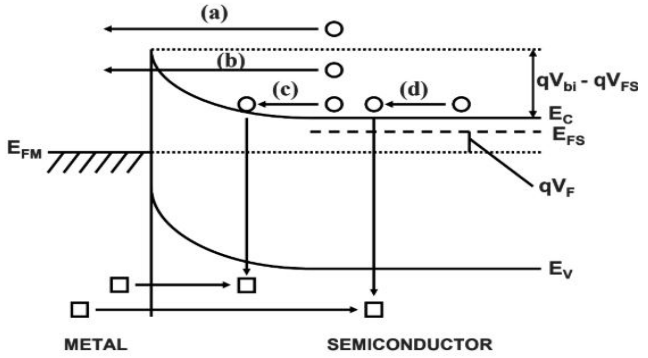


Fig. 2- Basic Schottky design
Adapted from *Fundamentals of Power Semiconductor Devices* (14), By B.J. Baliga, 2008, New York City, 2008

- **Doping concentration and drift region**
- **Potential gradient and Electric field**
- **Avalanche breakdown and impact ionization**



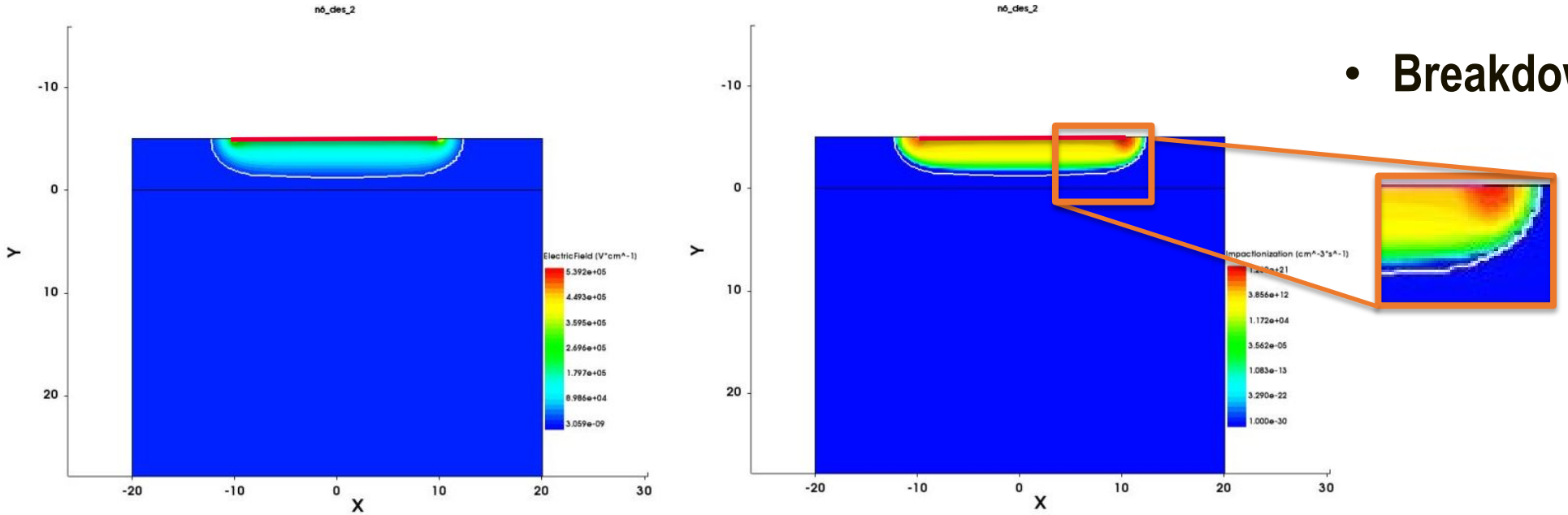
OFF State



ON State

Fig.3 Band Structure of a Schottky Diode
Adapted from *Fundamentals of Power Semiconductor Devices* (172), By B.J. Baliga, 2008, New York City, 2008

Circular Schottky Diode



- **Breakdown at 40V**

Fig. 4- Circular Diode impact ionization simulation

- Added field plate and passivation layer to reduce Electric field crowding at edges

Simulation Process

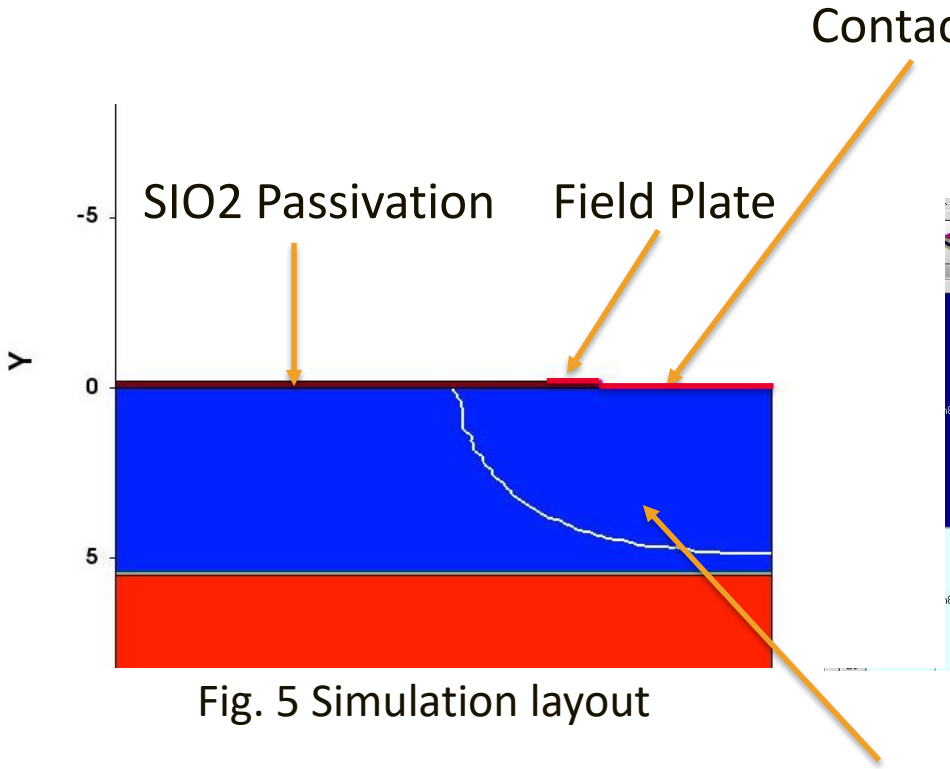


Fig. 5 Simulation layout

Device Design

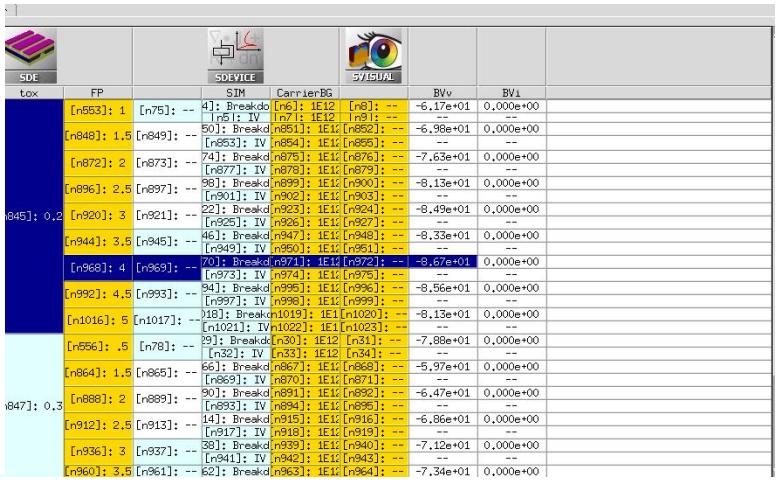


Fig. 6 Simulation split

Simulation Split

Field plate size →

Device size ↓

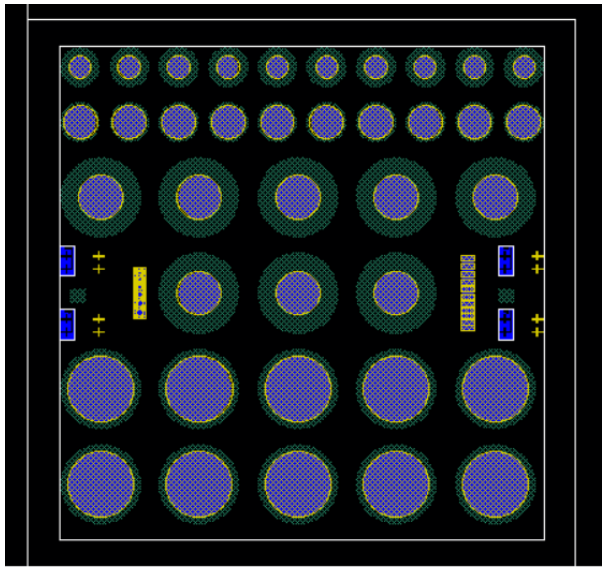


Fig. 7 Mask layout

Mask Layout

Si Epi Wafer Specification

Parameters	Value	Unit
Diameter	4	inch
Type	N^-/N^+	-
Dopant P	Phosphorous / Antimony	-
Epitaxy Thickness	4.70-5.75	um
Epitaxy Resistivity	1.120-1.380	ohm-cm
Epitaxy Concentration	~$3.5x10^{15}$	cm^{-3}
Substrate Resistivity	$0.554x10^{-3}$	Ohm-cm
Substrate Concentration	~$5x10^{19}$	cm^{-3}
Wafer Thickness	555	um

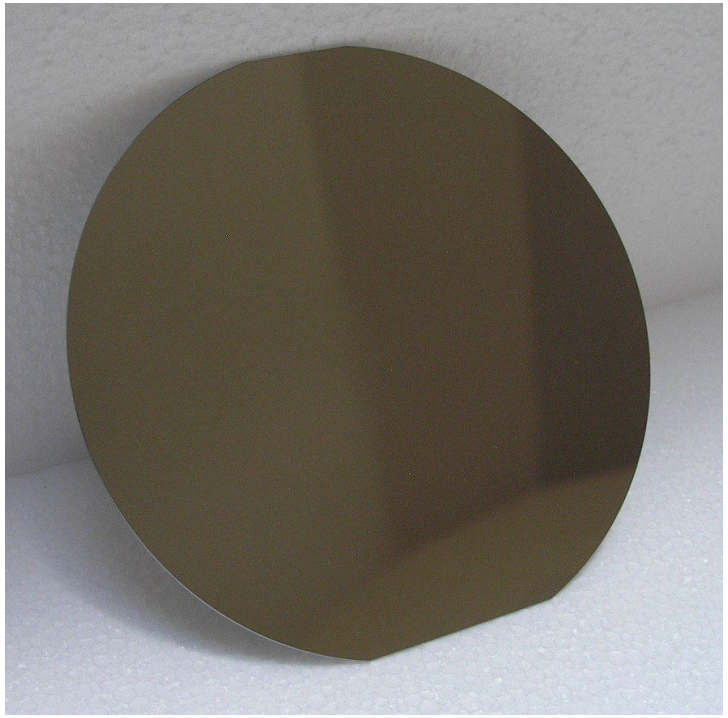
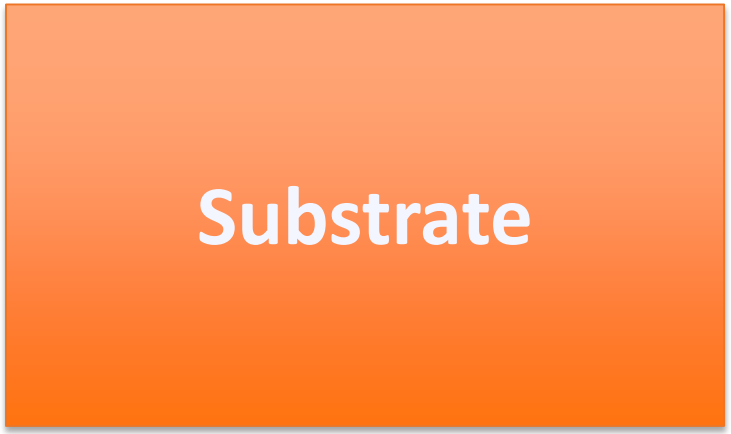


Fig. 8- 4’’ Epi Wafer

Fabrication Process Flow

Isolation Positive Photo (AZ1518)	Stock Positive Photo Resist
Si Isolation Etch Trion Oracle Etcher	CF4+O2 Gas Mixture to etch 0.2um
SiO_2 Deposition PECVD	0.2um deposition + thickness check with ellipsometry
Contact Open Positive Photo (AZ5209)	Stock Thin Negative Photo Resist used as Positive for higher resolution
Contact Open Etch BOE wet etch	SiO_2 wet etch using BOE dip
Ohmic Metal Deposition CHA #1	Ti = 150nm
Post Metal Deposition Annealing	450 ℃ 3min N2 Ambient
Schottky Negative Photo (AZ5209)	Negative Photo Resist for Metal Lift-Off
Schottky Metal Deposition CHA #1	Ni = 150nm
Post Metal Deposition Annealing	450 ℃ 10sec N2 Ambient



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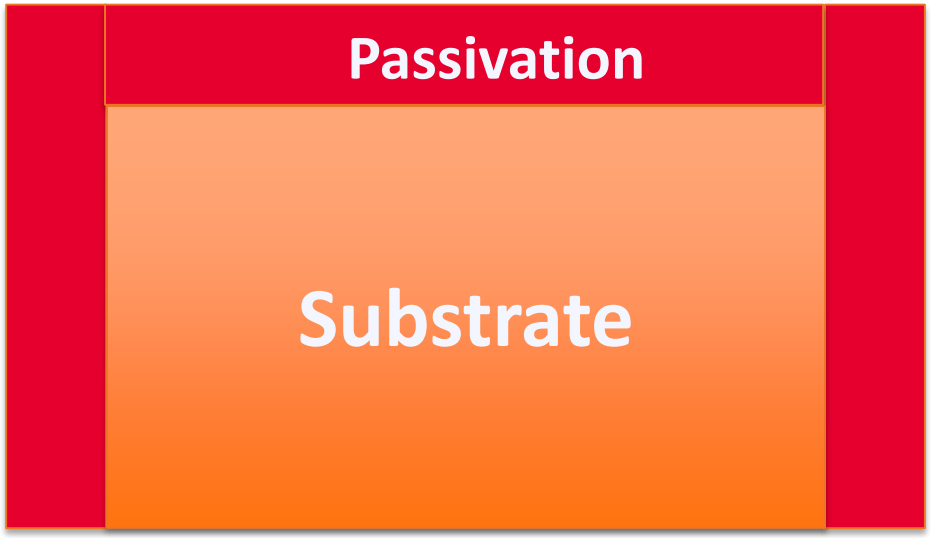

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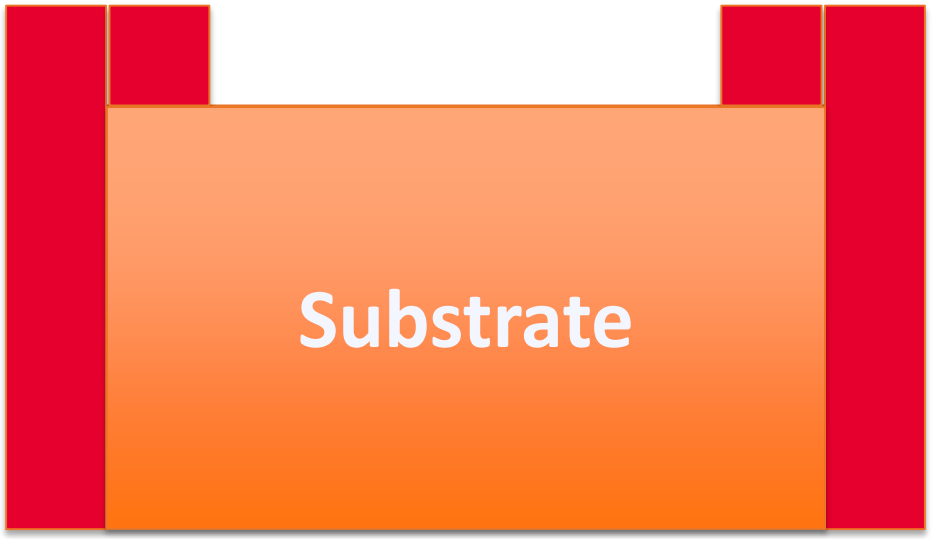

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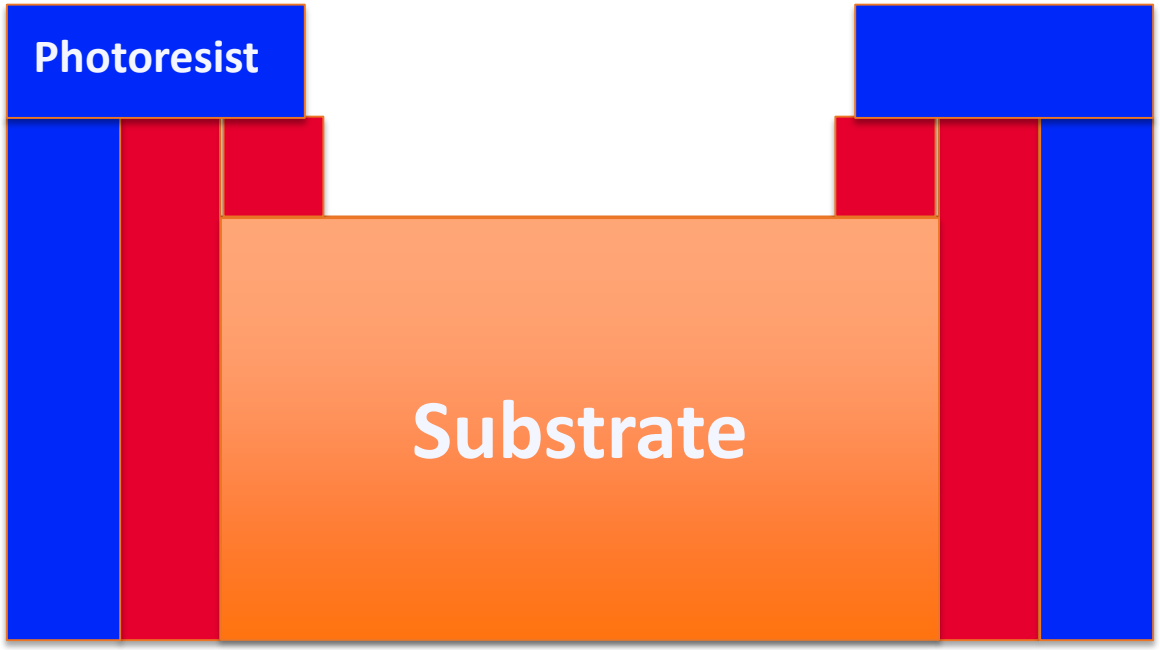

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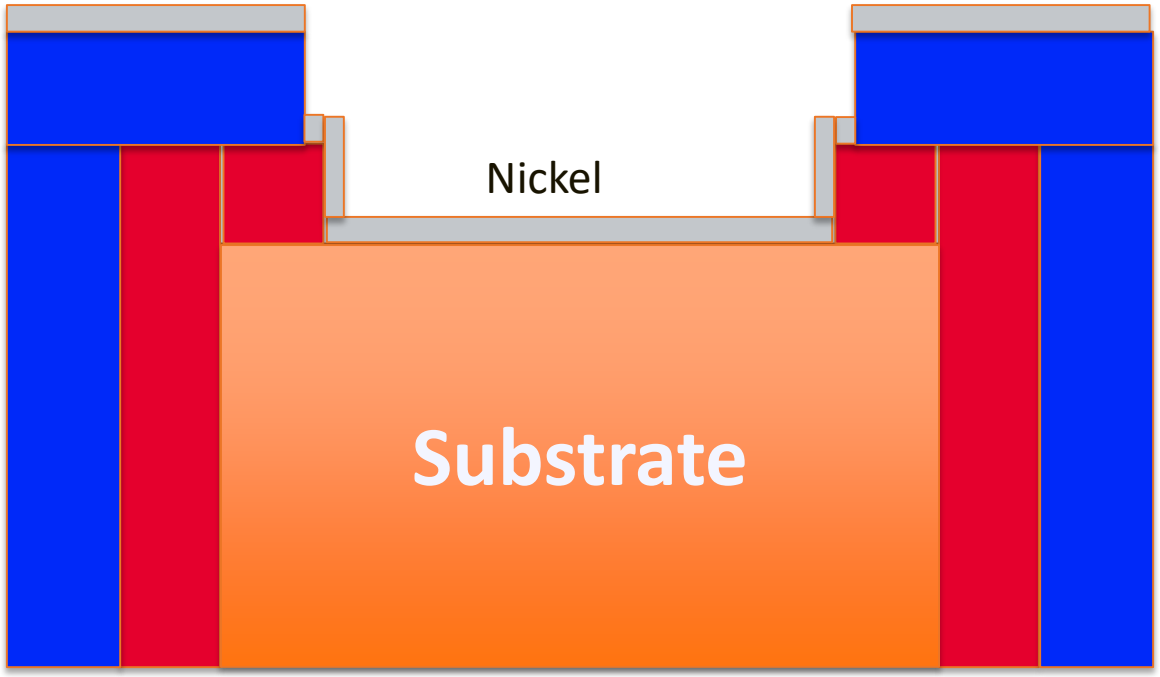

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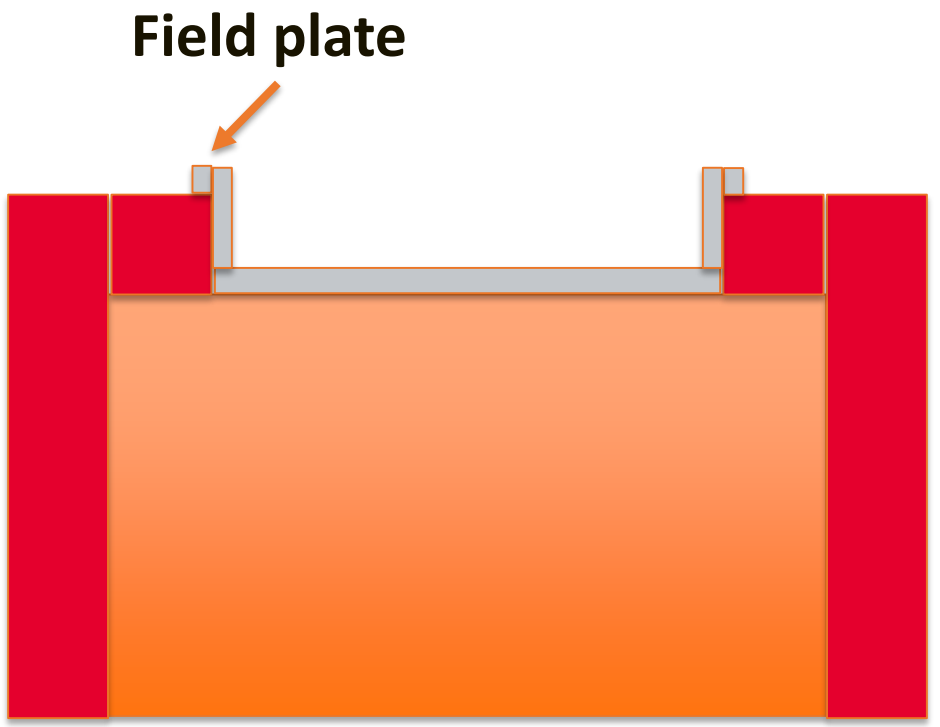

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Fabrication Process Images

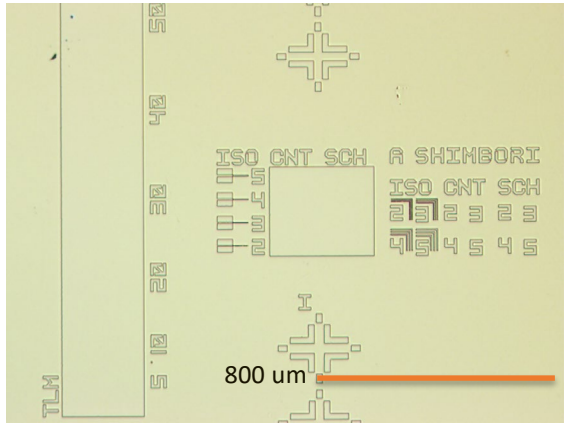

Fig. 9 Isolation alignment marks

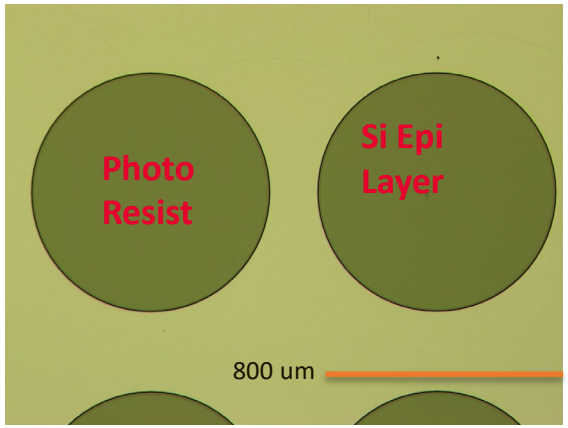

Fig. 10- Isolation photo

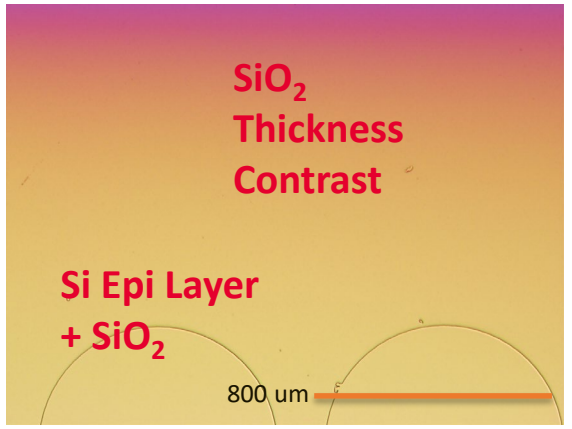

Fig. 11 Passivation

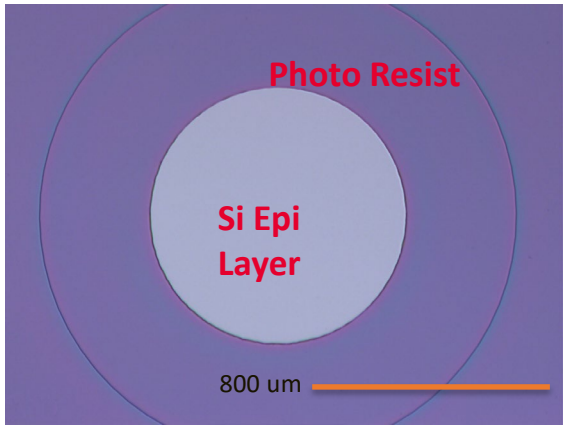

Fig. 12 Contact open photo

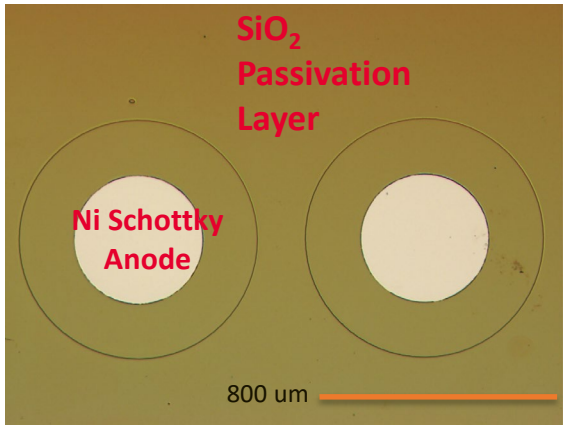

Fig. 13 Ni deposition

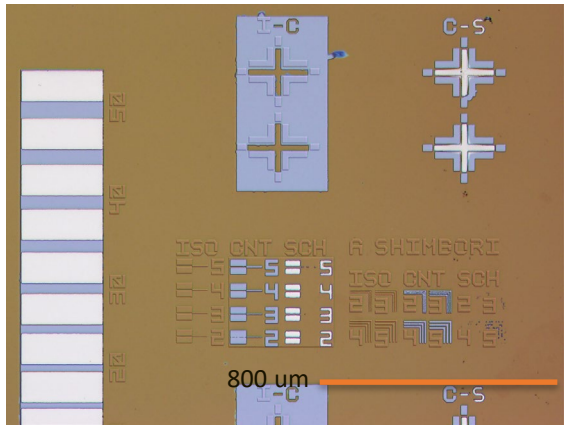

Fig. 14 Completed process alignment

Si Schottky with Field Plate Structure I-V Comparison

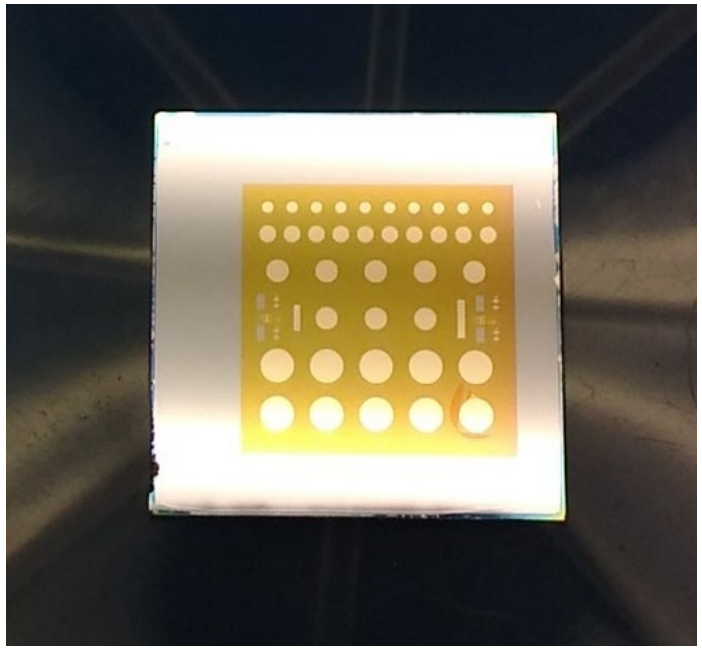

Fig.15 Final Fabricated Device

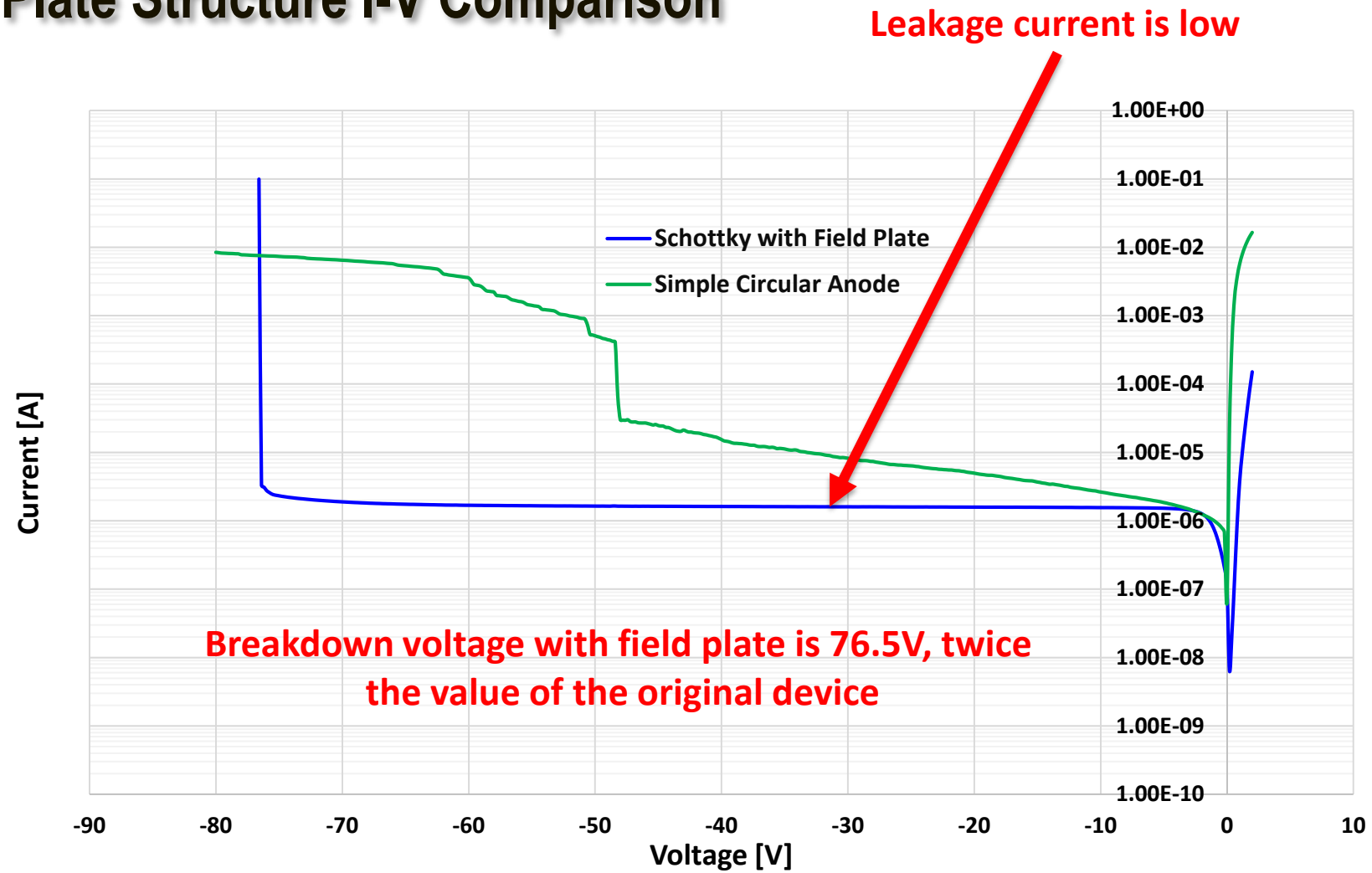

Fig. 16 IV curve final device vs. circular anode

Comparison of Forward I-V Characteristics

- Area doubles in each successive group
- On-Resistance (R = Pl/A)
  Type D<Type C< Type B< Type A

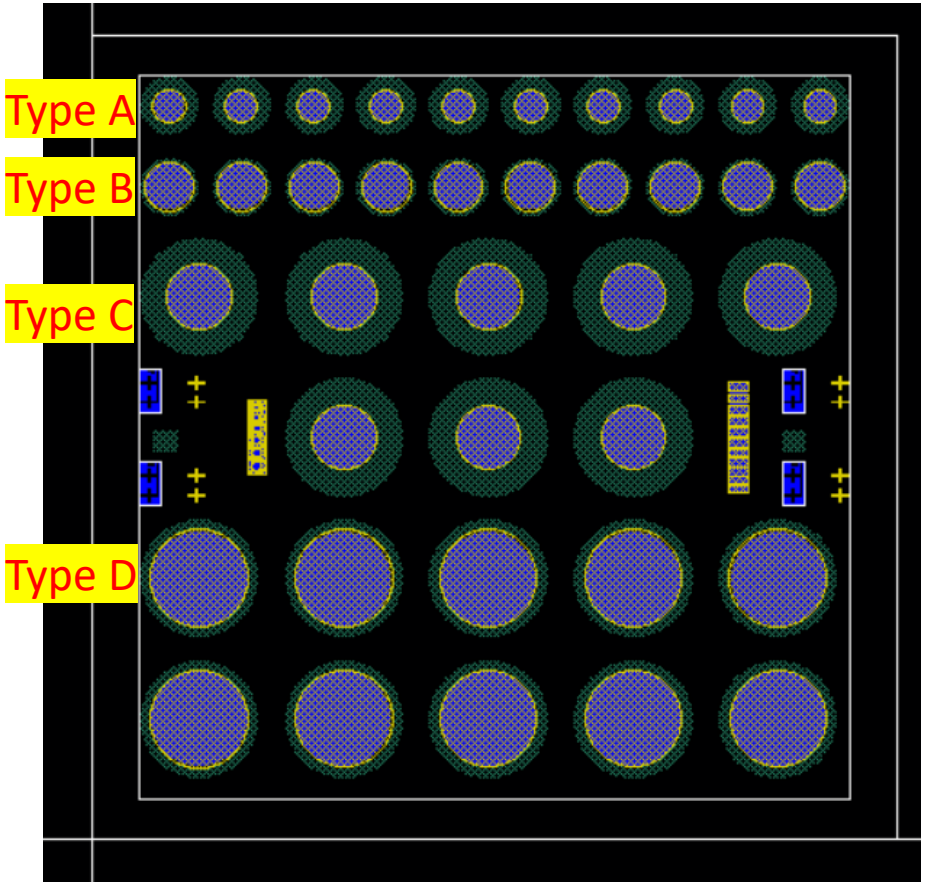

Fig.17 Mask Layout

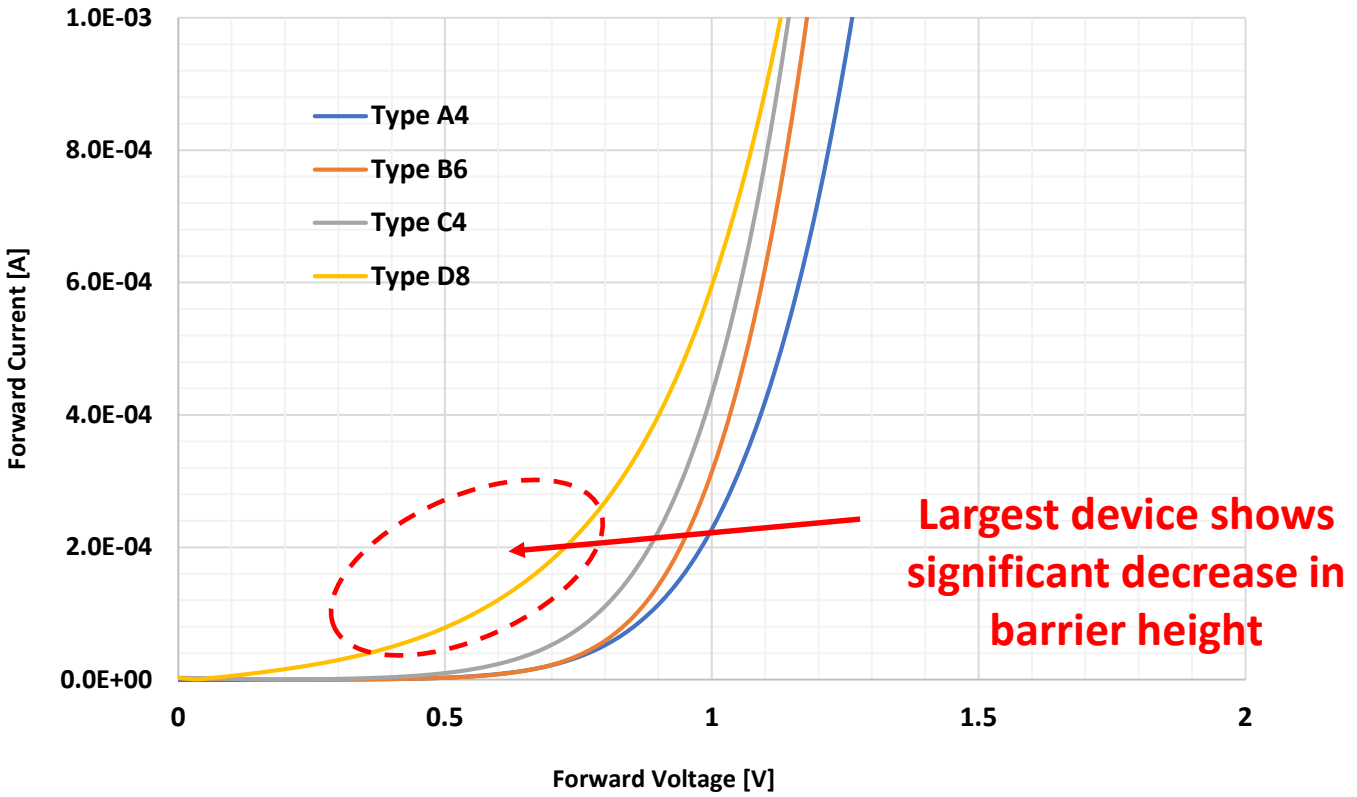

Fig.18 Forward voltage comparison

Conclusions

- SiO_2 passivation and field plate structure reduces electric field crowding at the anode contact edge.
- Breakdown voltage with the field plate structure is 2 times higher than the simple circular anode with a value of 76V
- SiO_2 passivation reduces surface leakage current