NNCI Computation

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National Nanotechnology Coordinated Infrastructure

Objectives

- To facilitate access to the modeling and simulation capabilities and expertise
- To promote and facilitate the development of new capabilities.
- To promote utilization of the computation resources.

Short Course on Electronic Device Modeling

SDMS: Semiconductor Device Modeling and Simulation

By Dragica Vasileska

Electrical, Computer and Energy Engineering Arizona State University, Tempe AZ

View Courses

Audio podcast
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1 question (Ask a question)
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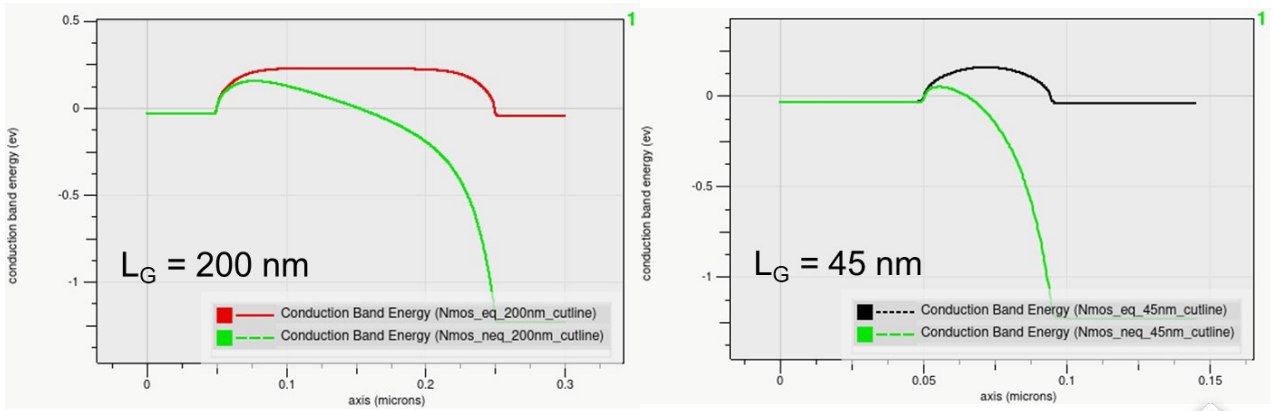

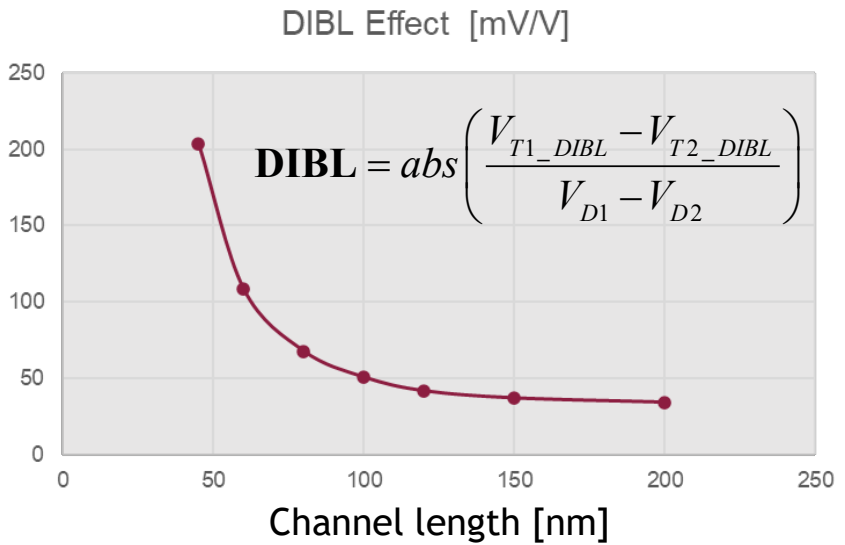

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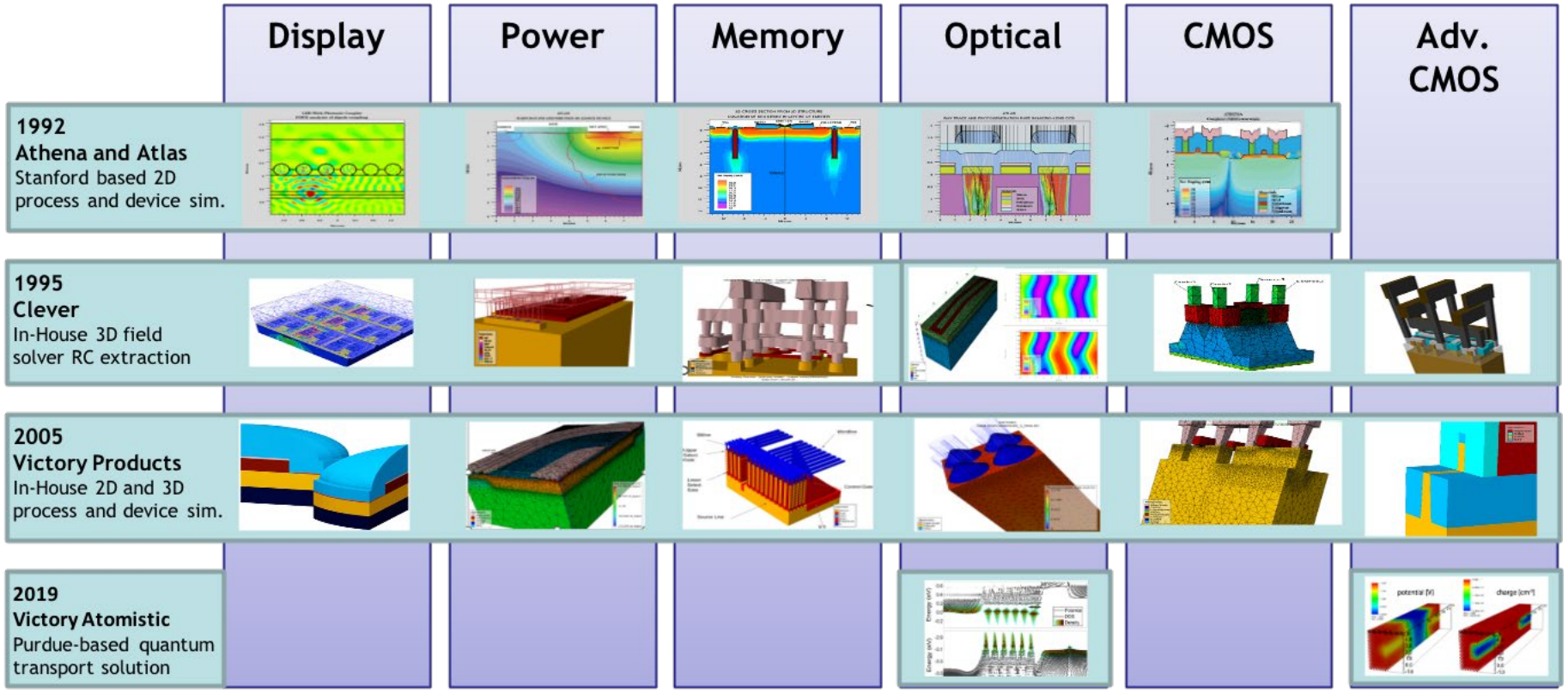
Silvaco Modeling Tools on nanoHUB



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Assignments are on NanoHUB – For Instructors

Basic Semiconductor Device Modeling with Tools on nanoHUB

By Dragica Vasileska

Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

View Courses

Audio podcast
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Slides/Notes podcast

176 users ⟷ Material released September 15, 2024

0 questions (Ask a question)
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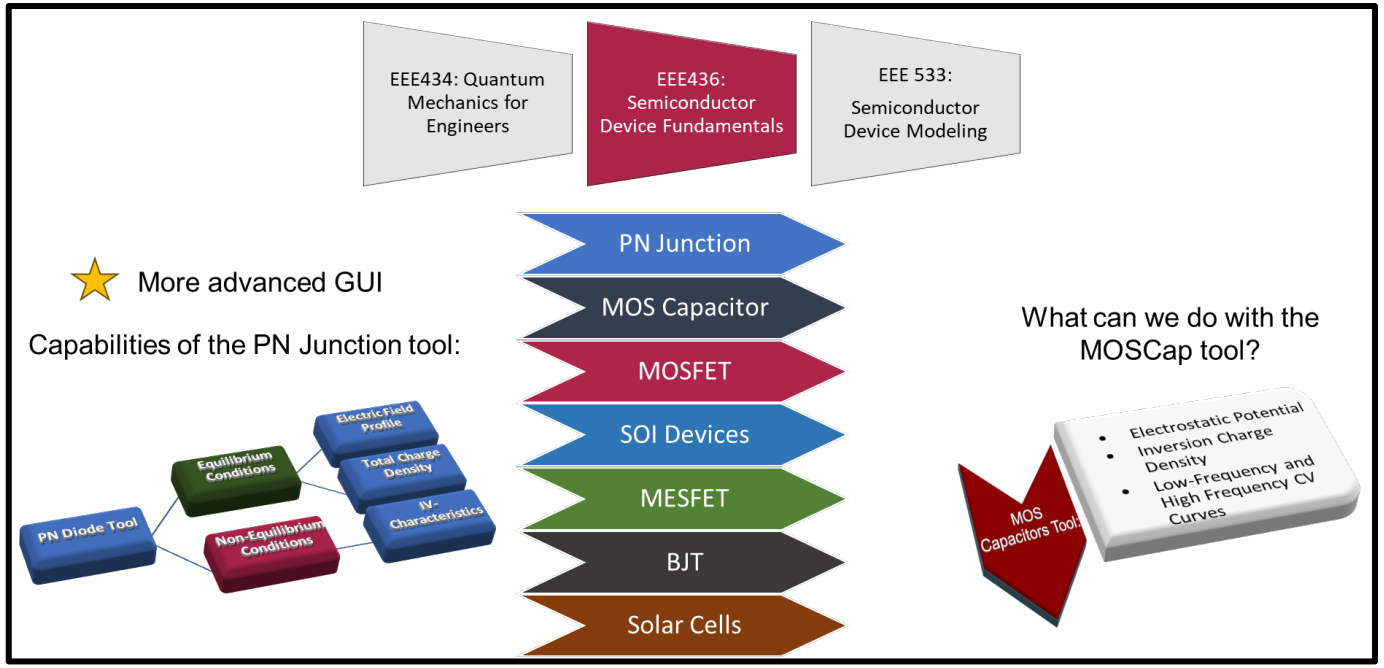

Example assignment:

Homework 3 – MOSFET Modeling

Objective

The objective of this set of problems is to understand MOSFET operation with gate lengths ranging from couple of micrometers to tens of nanometers. Standard description of the MOSFET device operation is presented first. We briefly discuss:

- ***Gradual channel approximation*** (square law and bulk charge theory) for long channel devices, and
- ***Velocity saturation model***, valid for nanoscale devices in which, due to the large electric fields, there is degradation of the electron/hole mobility.

The problems assignments address non-idealities of these models, which are called short-channel effects, such as threshold voltage roll-off, velocity saturation and the Drain Induced Barrier Lowering (DIBL) effect. This set of problems uses the MOSFET Lab that can be accessed via ABACUS toolkit: (https://nanohub.org/resources/abacus).

Theoretical Background

MOSFET is the most common field effect transistor in use today. The *gate* electrode is biased to produce an electric field that controls the conductivity of a "channel" between two terminals, called the *source* and *drain*. Depending on the type of carriers in the channel, the device may be an *n-channel* (for electrons) or a *p-channel* (for holes) MOSFET. The configuration, symbol and transfer characteristics for *n*-channel and *p*-channel enhancement (normally off) or depletion mode (normally on) devices are shown in Fig. 1.

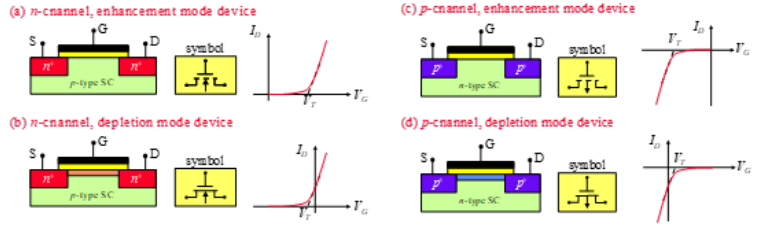

Figure 1. Cross-sectional diagrams, circuit symbols, and transfer characteristics of the four basic MOSFET configurations.

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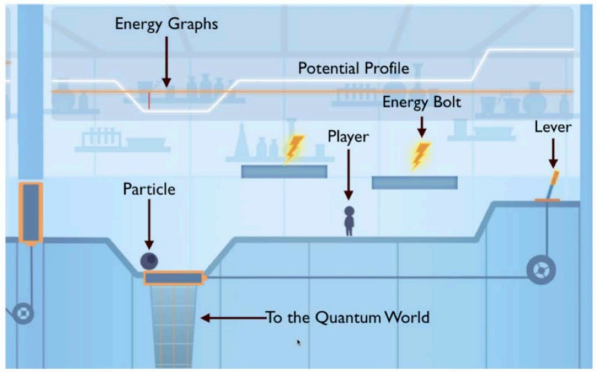
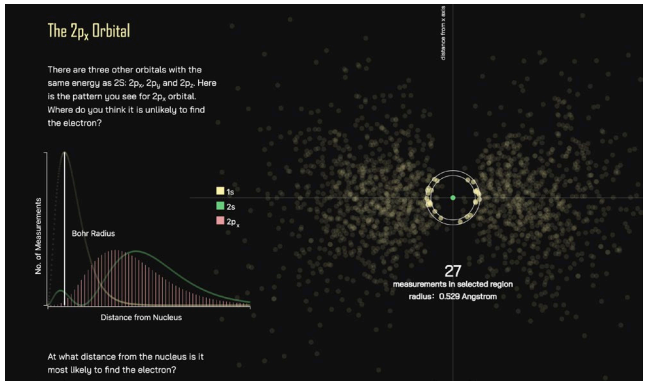
Solutions to these assignments available for **Instructors** upon request!

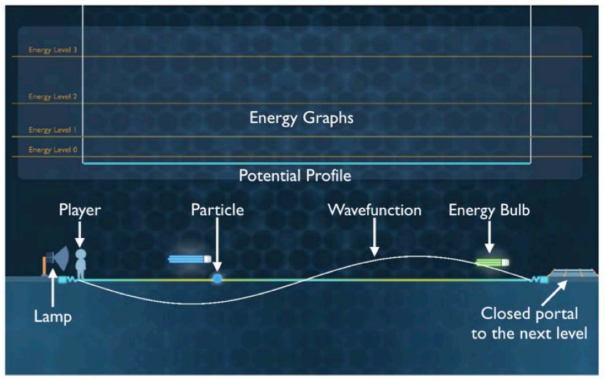
Immersive Virtual Worlds for Experiential Learning of Microelectronics

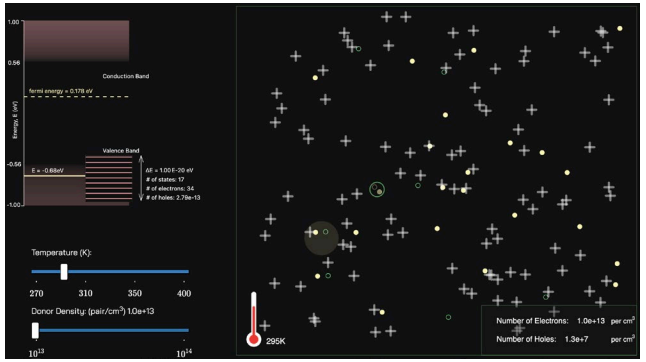


Immersive Games from Classic to Quantum Worlds



Interactive Visualizations from Hydrogen Atom to Carrier Statistics in Si





Interactive Visualizations and Virtual Reality for Semiconductor Devices

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NSF

https://learnqm.gatech.edu

Georgia Tech

Collaborative NSF Award

Program: Improving Undergraduate STEM Education (IUSE), Level 3

Title: Interactive Visualizations and Simulations for Conceptual Understanding in Quantum and Semiconductor Physics

Goals:

1) Enhance and Expand the educational tools for experiential learning of the semiconductor physics and devices.

2) Conduct large-scale evaluations of the tools with more than 350 students across 5 universities with very diverse populations.

3) Answer two major research Questions: To what extent can such tools change students' conceptions? and 2) How does the design of such tools affect students' conceptions?

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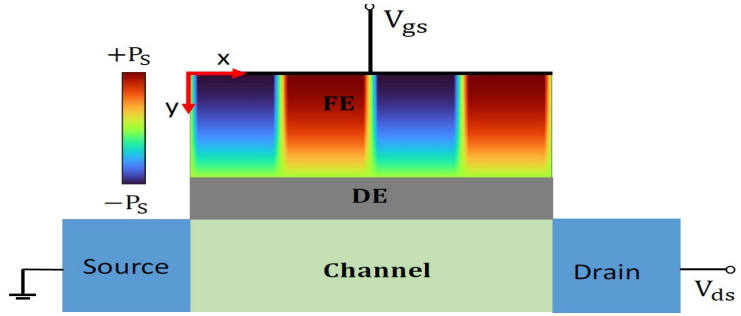
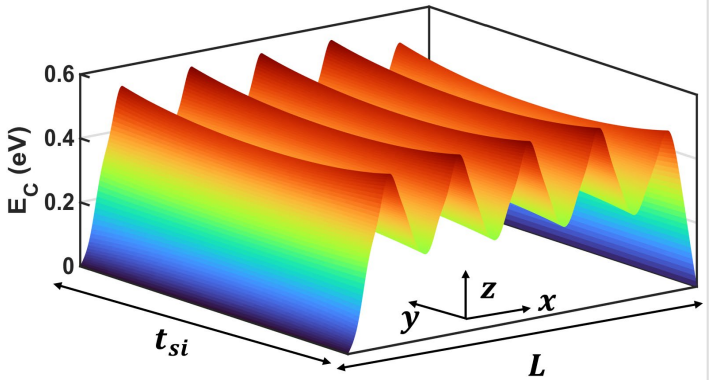
Phase-Field Modeling of Domain Formation in FeFETs

- Phase-field model developed in COMSOL.
- Coupled solution of 2-D Poisson's equation & Landau energy state
  - Captures multi-domain texture in the ferroelectric layer.
  - Impact of ferroelectric domain dynamics on the device's electrostatics and transport including substantial changes in gate and source to drain tunneling
  - Device design guidelines derived for optimizing performance (ON/OFF ratio, switching speed, etc.)

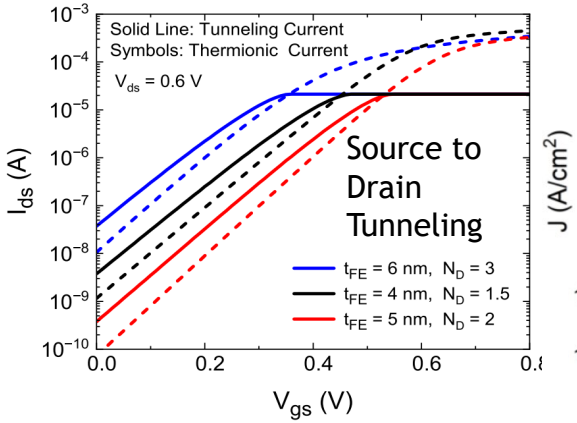


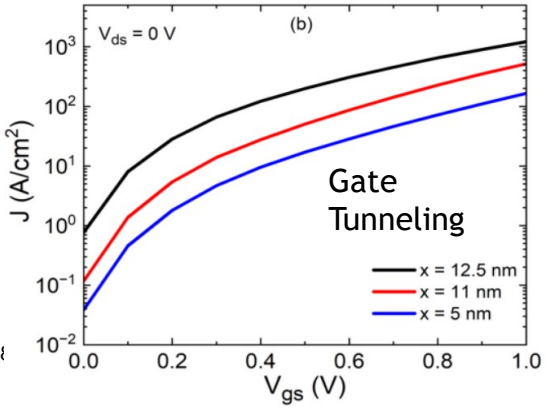


[1] N. Pandey, Y. S. Chauhan, L. F. Register, and S. K. Banerjee, "Dynamics of Domains and its Impact on Gate Tunneling in CMOS-Compatible FeFETs," IEEE Electron Device Letters, 2024, April 2024.

[2] N. Pandey, Y. S. Chauhan, L. F. Register and S. K. Banerjee, "Multi-Domain Dynamics and Ultimate Scalability of CMOS-Compatible FeFETs," in IEEE Electron Device Letters.

[3] N. Pandey, Y. S. Chauhan, L. F. Register, and S. K. Banerjee, "Impact of Multi Domain on Ferroelectric Tunnel Junction Design Metrics," 82nd Device Research Conference (DRC), Washington DC, USA, June 2024.





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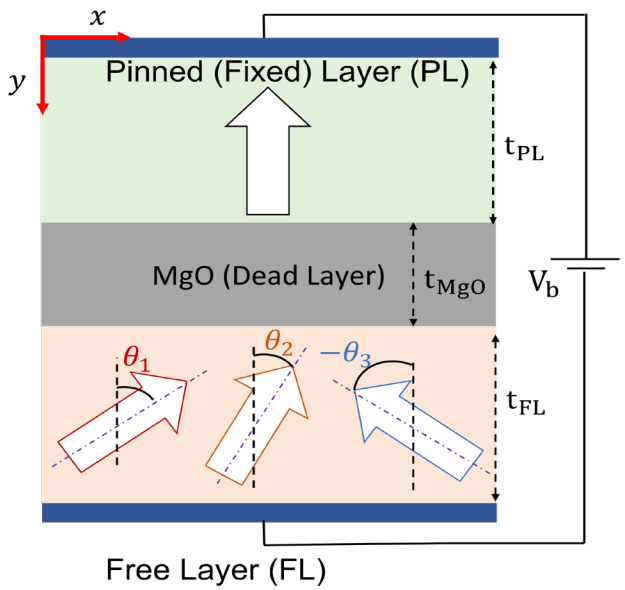
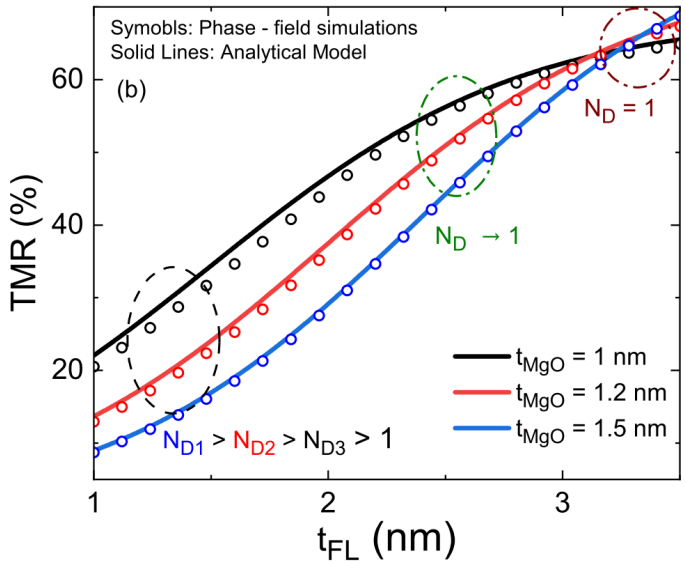
Phase-field Modeling of Multi-Domain Magnetic Tunnel Junctions

- Analytical model of magnetic tunnel junction derived by solving electrostatic Green's function
- Multi-domain impact on tunnel magnetic resistance (TMR) and switching speed analyzed.
- Basics of a compact model for circuit-level simulation derived.
- Phase-field models are being used to study and explain the experimental results in superconducting and 2-d FETs





[1] N. Pandey, Y. S. Chauhan, L. F. Register, and S. K. Banerjee, "2-D Analytical Modeling of the Magnetic Tunnel Junctions Including Multi-Domain Effects: Predictive Insights and Design Optimization," IEEE Transactions on Electron Devices, May 2024.

[2] N. Pandey, Y. S. Chauhan, L. F. Register, and S. K. Banerjee, "Impact of Multi-Domain Microscopic Interactions on Magnetic Tunnel Junction's Static and Transient Characteristics," 82nd Device Research Conference (DRC), Washington DC, USA, June 2024.

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SiGeSn Material System (muATOMS EFRC)

μATOMS

UAPB University of Arkansas at Pine Bluff — Mansour Mortazavi

The George Washington University, Washington, DC — Tianshu Li

SLAC National Accelerator Laboratory

Stanford University — Paul McIntyre

Sandia National Laboratories — Ezra Bussmann, Tzu-Ming Lu, Shashank Misra, Mike Lilly

University of Arkansas — Shui-Qing Yu, Hugh Churchill, Jin Hu, Hiro Nakamura, Greg salamo

University of Delaware — Yuping Zeng

Dartmouth — Jifeng Liu

Berkeley, University of California — Berkeley Lab — Andrew Minor

Yong-Hang Zhang, Dragica Vasileska — Arizona State University

Rensselaer — Shengbai Zhang

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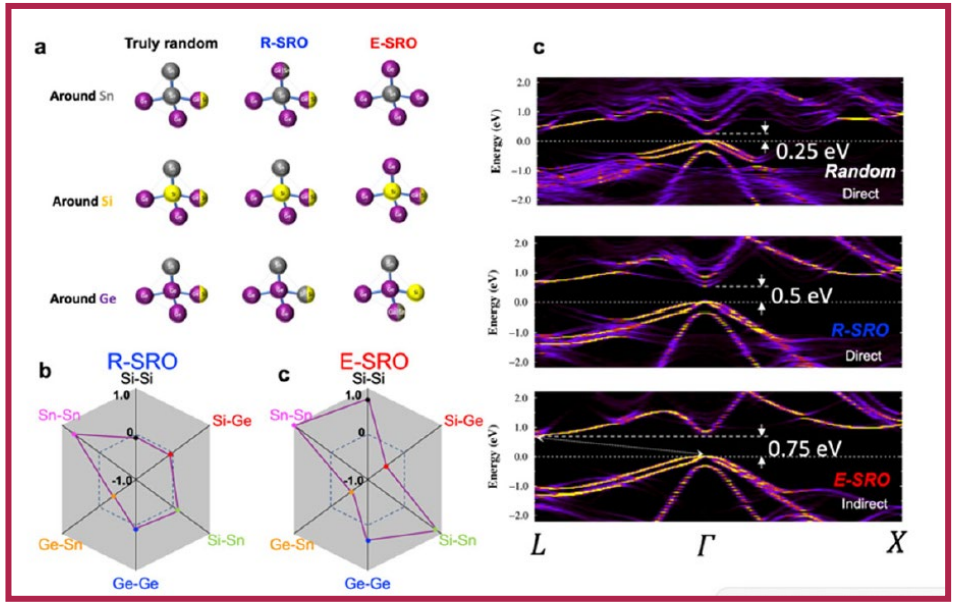
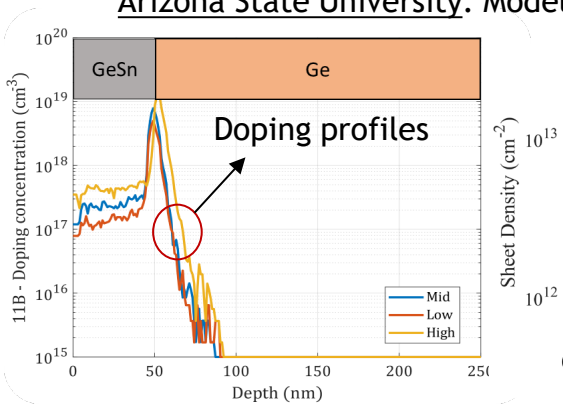
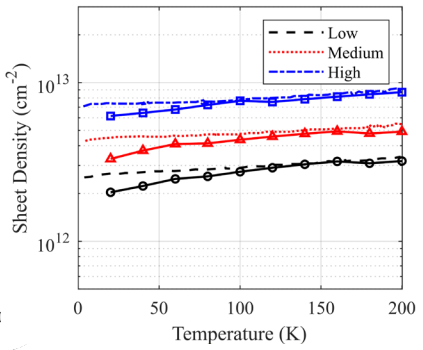
Short-Range Order: Another Degree of Freedom for Material Design

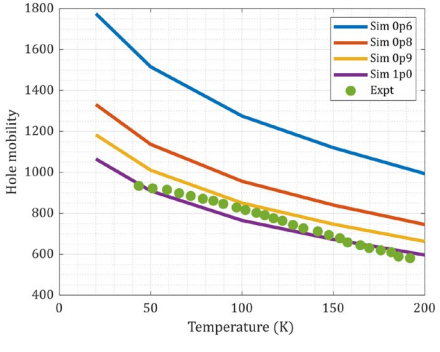


Sandia National Lab: Experimental characterization of GeSn/Ge heterostructures

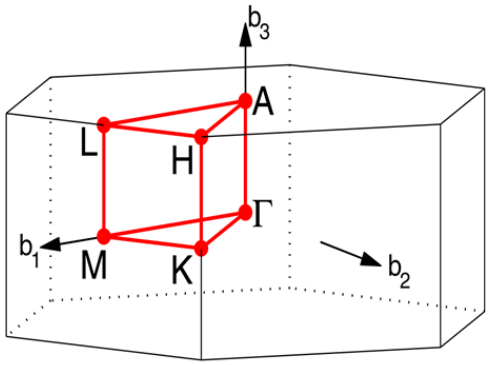
Arizona State University: Modeling of Hole transport in these heterostructures



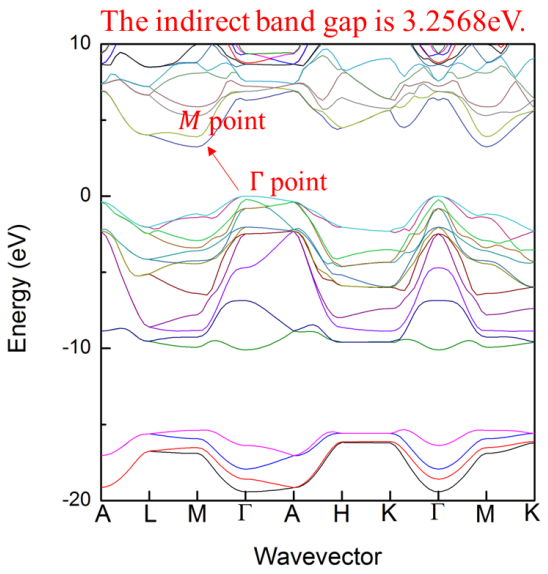


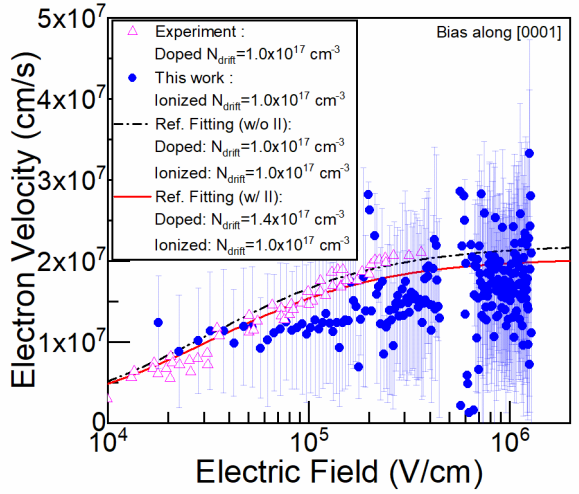


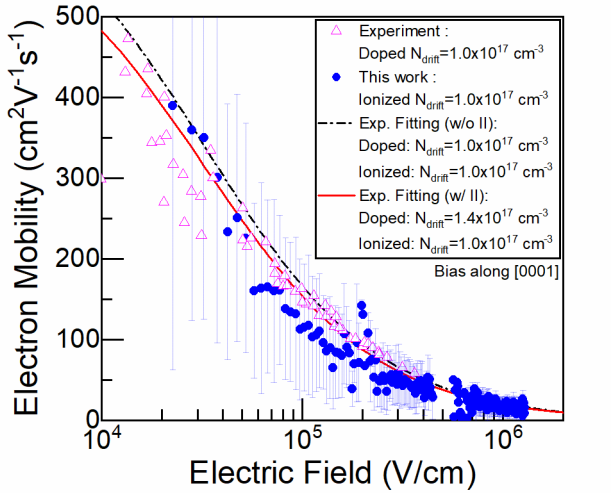
Wide bandgap devices: Modeling of 4H SiC VDMOS

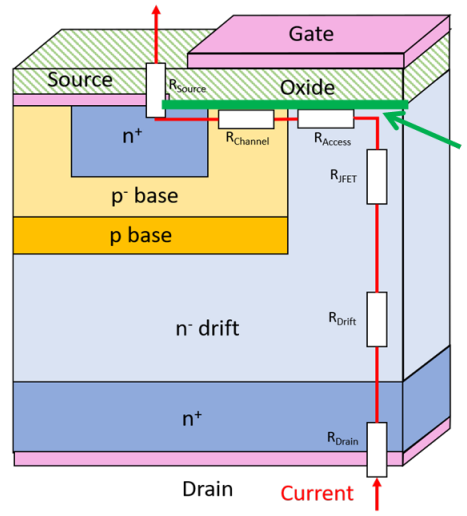


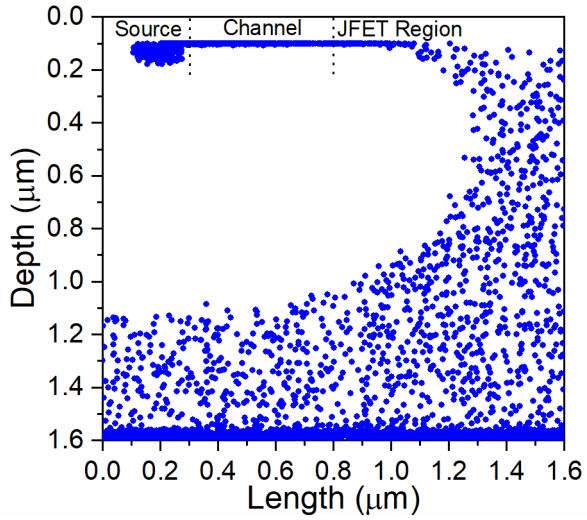
3D **Full-band** MC device simulator with **real-space treatment of the E-E and E-I interactions.**











- G. Ng, D. Vasileska and D. K. Schroder, Empirical pseudopotential band structure parameters of 4H-SiC using a genetic algorithm fitting routine, Superlatt. Microstructures 49(1), pp. 109-115 (2011).
- Chi-Yin Cheng and Dragica Vasileska, "Electron transport analysis of 4H-SiC with full-band Monte Carlo simulation including real-space Coulomb interactions", *Journal of Applied Physics* **127**, 155702 (2020).
- Chi-Yin Cheng and Dragica Vasileska, "Static and Transient Simulation of 4H-SiC VDMOS Using Full-Band Monte Carlo Simulation That Includes Real-Space Treatment of the Coulomb Interactions", *IEEE Trans. Electron Devices*, Volume: 67, Issue: 9, pp. 3705-3710, 2020.

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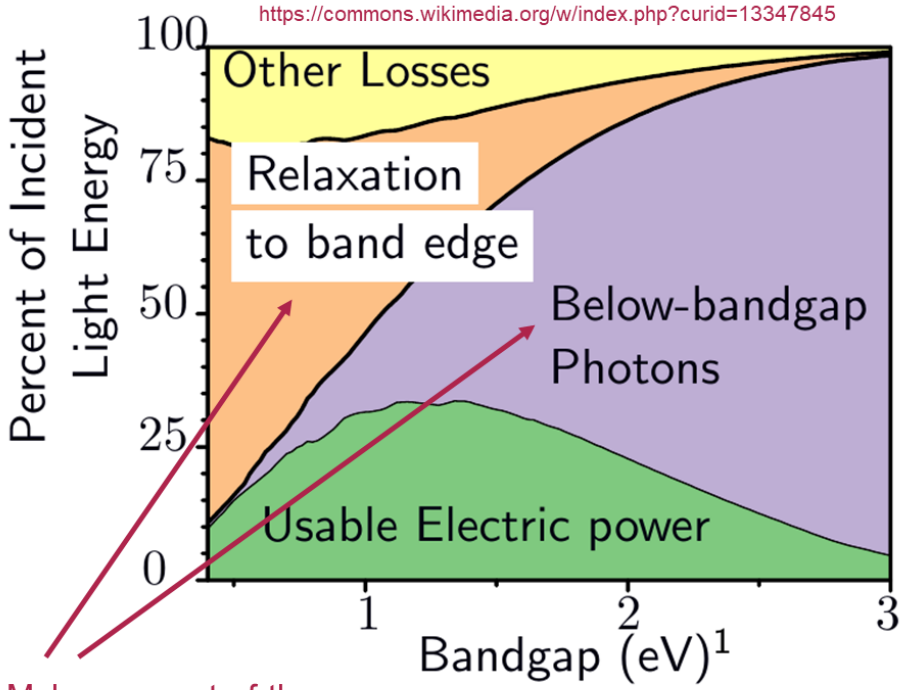
Modeling of Hot Carriers Solar Cells (S. M. Goodnick / D. Vasileska)



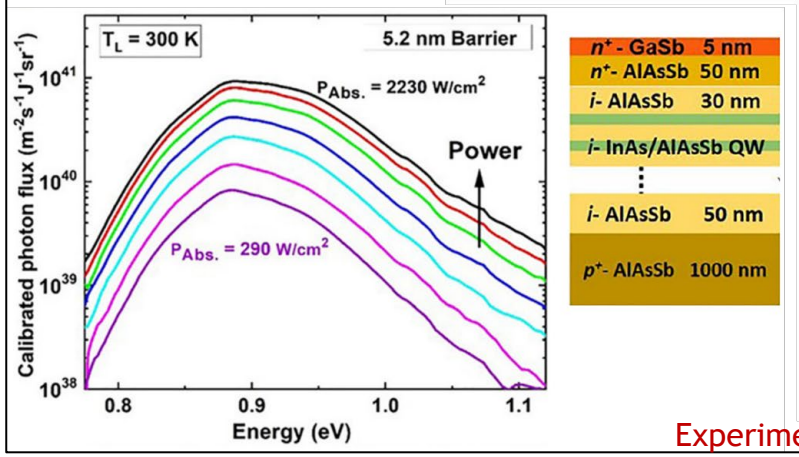
Make up most of the losses in SQ limit

If the relaxation to the band edges is prevented, efficiency of the cell can be increased

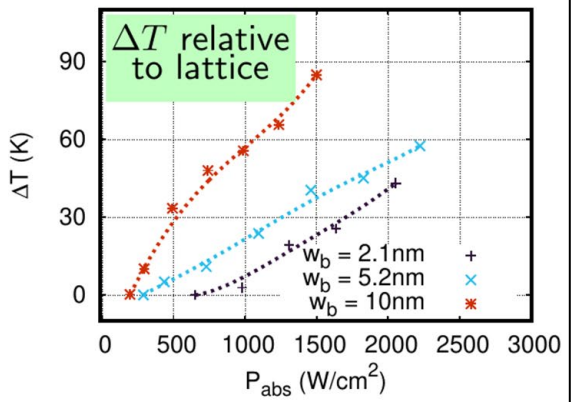
➔ **HOT CARRIERS SOLAR CELL**

Fit to generalized Plank's law

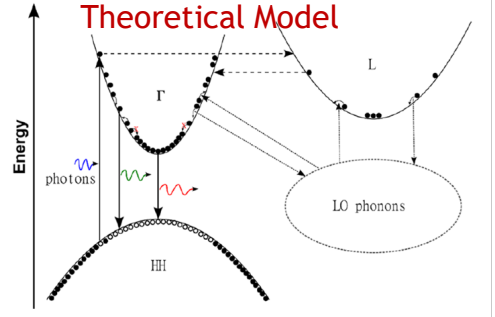
$$I_{PL}(E) = \frac{2\pi A(E) E^2}{h^3 c^2} \left[\exp\left(\frac{E-\Delta\mu}{k_B T} - 1\right)\right]^{-1}$$



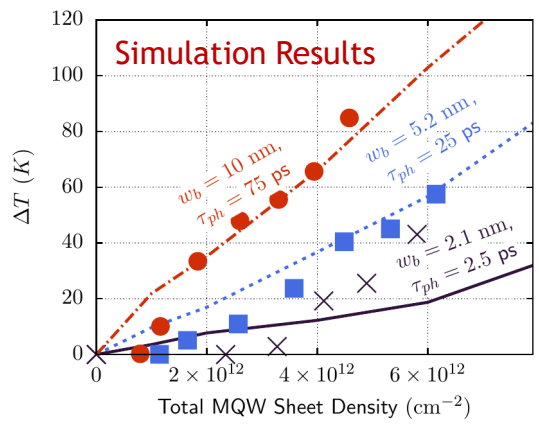
Experiment



Experimental proposal for Hot Carriers solar cell



$$\Delta T = T_e - T_L$$



- Scattering Mechanisms
  - Carrier-Carrier (e-e, e-h, h-h)
  - Degeneracy
  - Phonons:
    - Acoustic
    - Inter/intraband
    - inter/intravalley
    - Non-equilibrium polar-LO
- Relaxation of LO phonons modeled with: $\frac{\partial N(\mathbf{q})}{\partial t} = -\frac{1}{\tau_{LO}}\left(N(\mathbf{q}) - N_0(\mathbf{q})\right)$
- Coupled EMC to self-consistent Schrödinger-Poisson and empirical fit for generation/recombination rate

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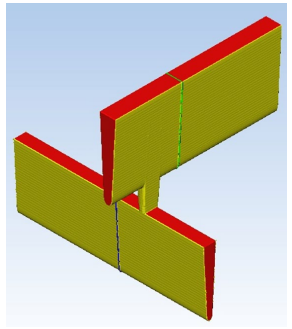
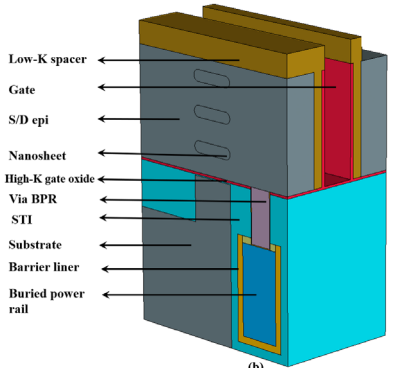
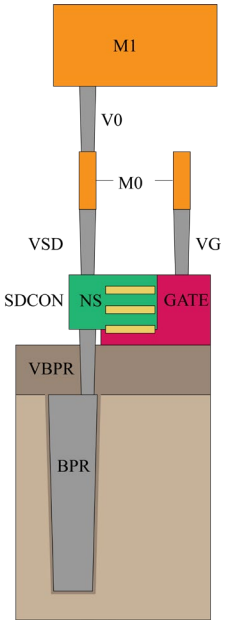
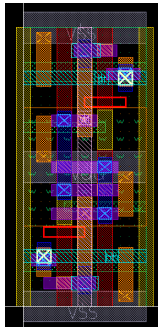
3nm Nanosheet GAA-FET Process Design Kit

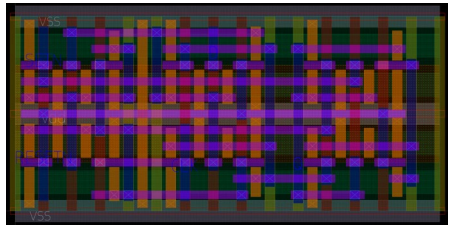




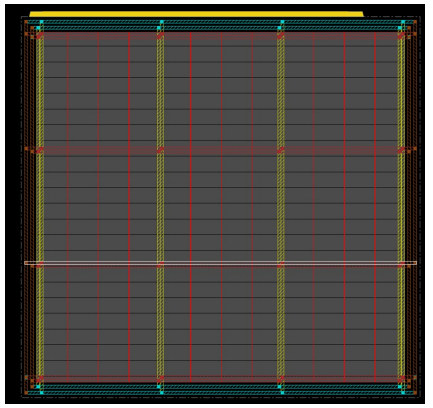


Interconnect and Transistor TCAD and Process Simulations

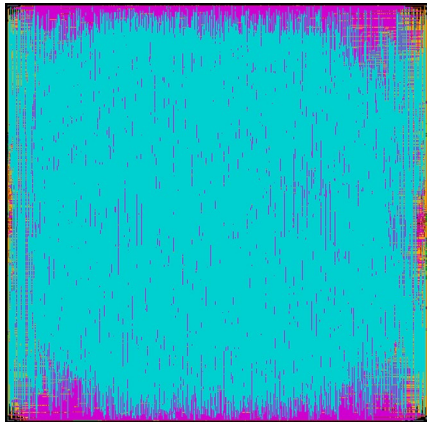




Standard Cell Library Design and Characterization (~ 60 cells)



BEOL Definition and Characterization



Place and Route

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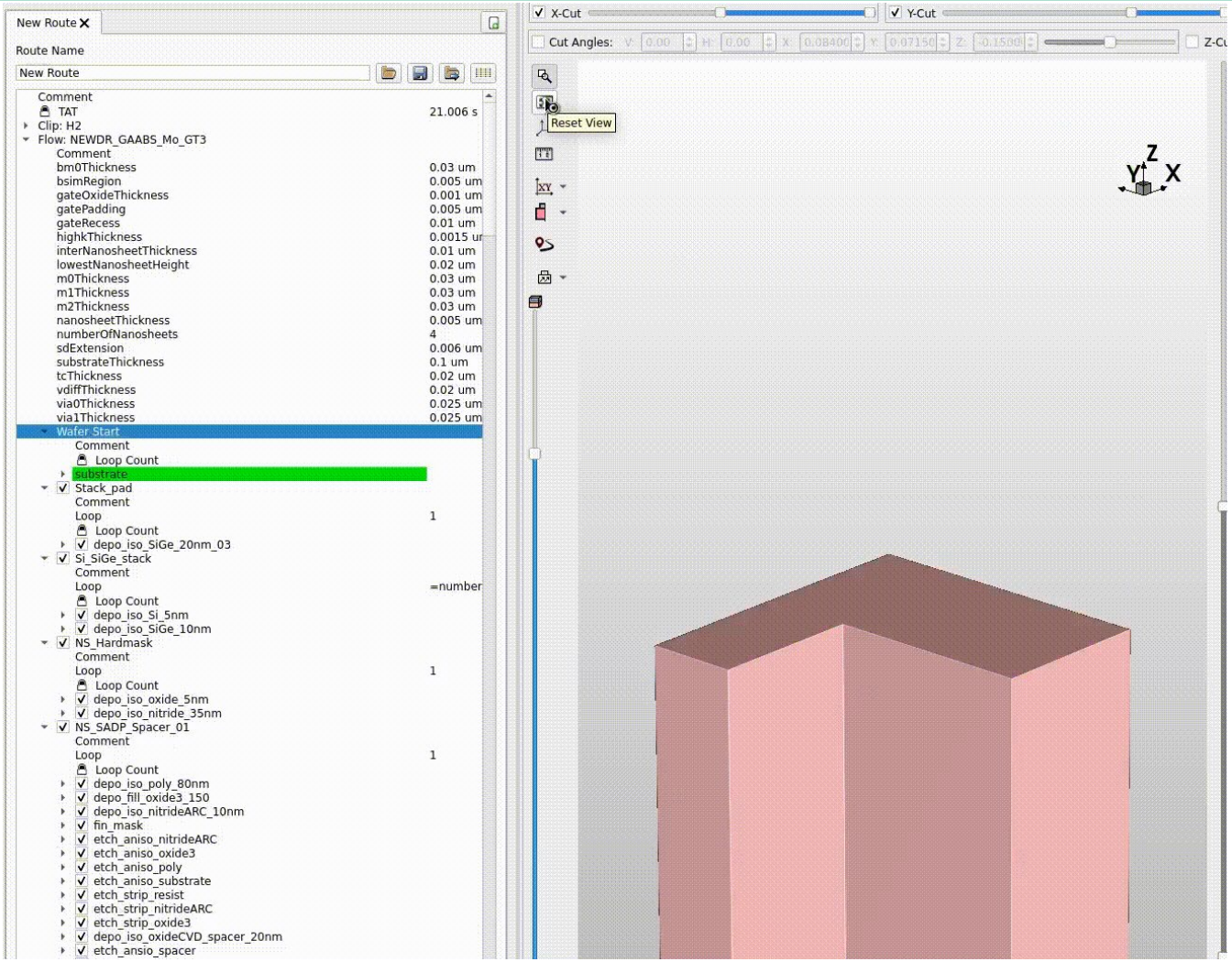
Semiconductor Research Corporation

CoCoSys
CENTER FOR THE CO-DESIGN OF COGNITIVE SYSTEMS

Collaboration with Synopsys: Process Emulations



Collaboration with Drs. Victor Moroz, Alexei Svizhenko, and Joanne Huang from Synopsys

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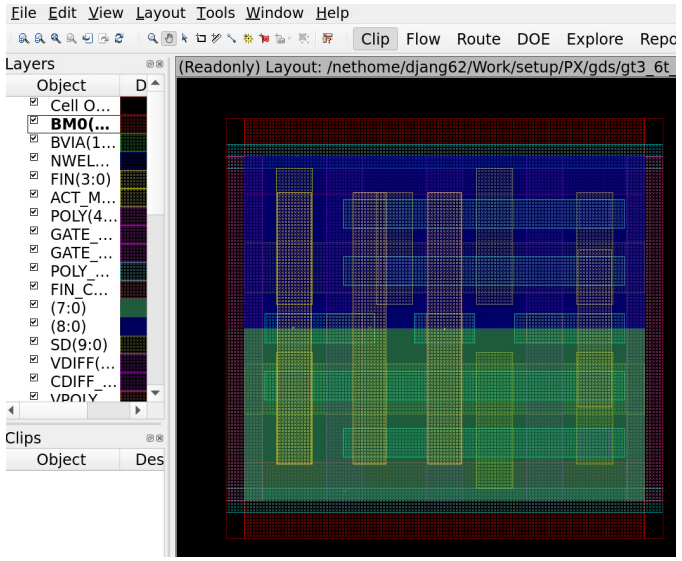
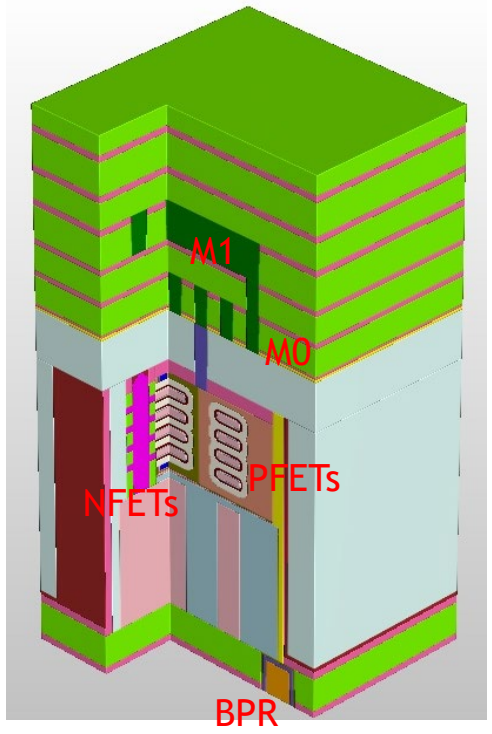
3nm Nanosheet GAA-FET PDK Development



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*|CAPACITANCE GRAND_SUM 1.3577e-04PF
*|A VDD 3.1506e-05PF
*|A VSS 3.1488e-05PF
*|A Y 5.7189e-05PF
*|VDD VSS 6.0180e-06PF
*|VDD Y 4.7846e-06PF
*|VSS Y 4.7846e-06PF

*|NET A 1.2018e-04PF
C_0_0 A VDD:LM10TungstenXG87ULM130Copper3XG66X1 9.2207e-24
C_0_1 A VDD:LM10TungstenXG87ULM90TiSiXG90X1 4.2152e-19
C_0_2 A VDD:p1s_1 4.6865e-21
C_0_3 A VDD:p2s_2 1.4454e-24
C_0_4 A VDD:p3s_3 4.7802e-24
C_0_5 A VSS:LM10TungstenXG34ULM130Copper3XG57X1 9.5252e-24
C_0_6 A VSS:LM10TungstenXG34ULM90TiSiXG33X1 4.2149e-19
C_0_7 A VSS:n1s_1 4.7116e-21
C_0_8 A VSS:n2s_2 1.4551e-24
C_0_9 A VSS:n3s_3 4.7931e-24
C_0_10 A Y:LM10TungstenXG171ULM150CobaltXG36X1 3.2588e-20
C_0_11 A Y:LM10TungstenXG171ULM90TiSiXG176X1 9.4320e-20
C_0_12 A Y:LM10TungstenXG172ULM150CobaltXG173X1 3.2650e-20
C_0_13 A Y:LM10TungstenXG172ULM90TiSiXG177X1 9.4332e-20
C_0_14 A Y:LM110MolybdenumXG140ULM120MoXG170X1 1.0394e-18
C_0_15 A Y:LM110MolybdenumXG169ULM120MoXG44X1 7.5439e-18
C_0_16 A Y:LM110MolybdenumXG41ULM120MoXG44X1 1.0389e-18
C_0_17 A Y:n1d_1 3.1504e-21
C_0_18 A Y:n2d_2 8.8140e-24
C_0_19 A Y:n3d_3 1.6702e-23
C_0_20 A Y:p1d_1 3.1445e-21
C_0_21 A Y:p2d_2 8.7016e-24
C_0_22 A Y:p3d_3 1.6630e-23
C_0_23 A:LM110MolybdenumXG47ULM120MoXG86X1 VDD:LM10TungstenXG87ULM130Copper3XG66X1 8.7444e-25
C_0_24 A:LM110MolybdenumXG47ULM120MoXG86X1 VDD:LM10TungstenXG87ULM90TiSiXG90X1 6.8652e-20
C_0_25 A:LM110MolybdenumXG47ULM120MoXG86X1 VDD:p1s_1 1.1020e-21
C_0_26 A:LM110MolybdenumXG47ULM120MoXG86X1 VDD:p2s_2 3.7648e-25
```

3nm GDS layout with appropriate layer assignments

Foundry 3nm fabrication process emulated by Process Explorer

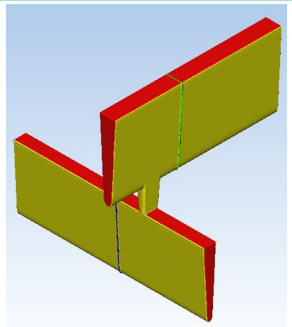
Raphael FX extracts overall parasitic RC netlist (.spf).

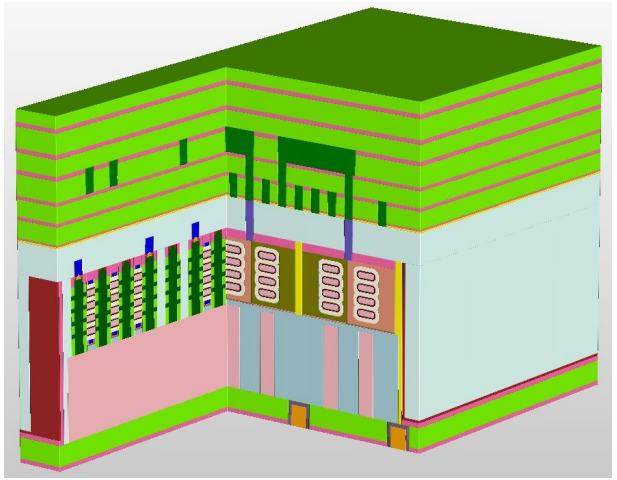
Process-aware cell library generation!

National N Coordinated Infrastructure

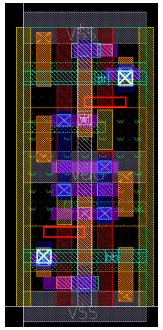
CoCoSys
CENTER FOR THE CO-DESIGN OF COGNITIVE SYSTEMS

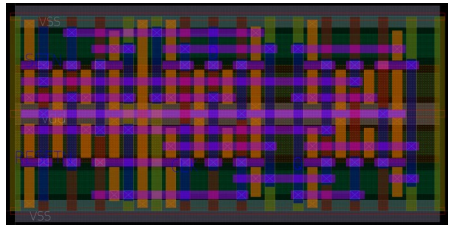
DTCO: TCAD to Full Chip



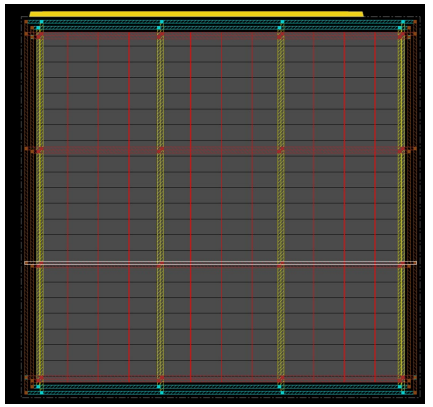


Process Aware TCAD Simulations

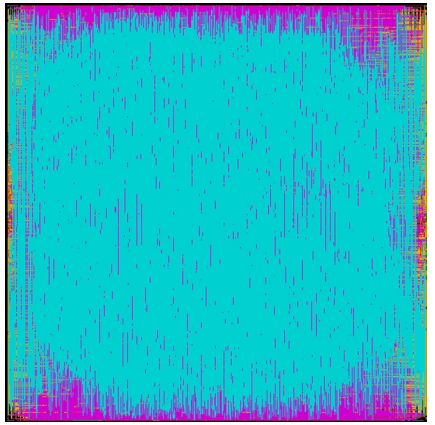




Standard Cell Library Design and Characterization (~ 60 cells)



BEOL Definition and Characterization



Place and Route

National Nanotechnology Coordinated Infrastructure

NSF

CoCoSys
CENTER FOR THE CO-DESIGN OF COGNITIVE SYSTEMS

Summary

- Short Course on Electronic Device Modeling
- Immersive Virtual Worlds for Experiential Learning of Microelectronics
- Physical modeling for FeFETs, MTJs, SiGeSn material systems, SiC VDMOS, and Hot Carrier Solar Cells.
- Open Source PDK for the 3nm nanosheet CMOS Technology