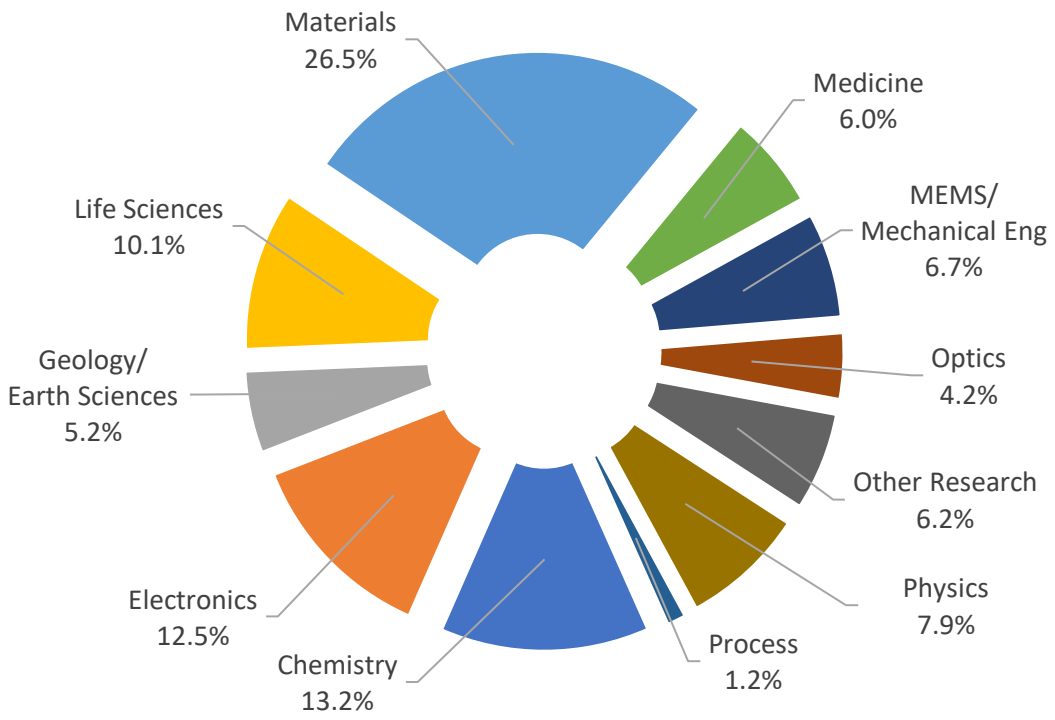
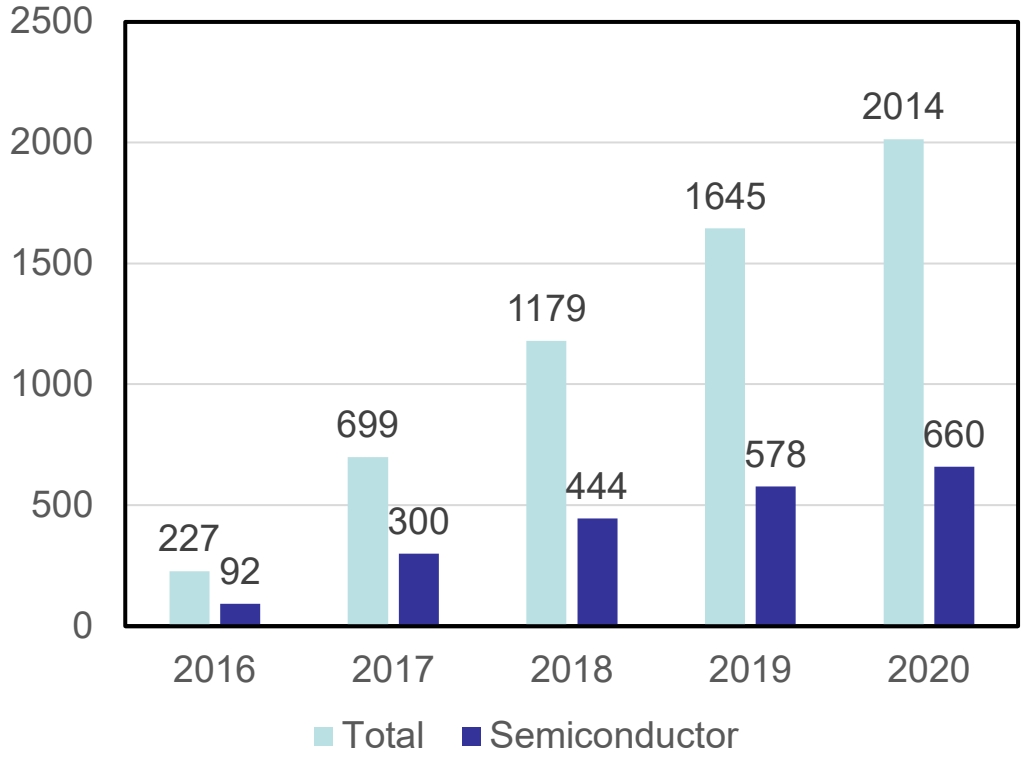
Semiconductor Research Supported by NNCI (2020)





33-43% of all research related to Microelectronics
Source: NNCI and Semiconductor Research Report, Oliver Brand and David Gottfried, March 2021

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Microelectronics Commons Workshop, Sept. 8, 9 2022

1) Semiconductor R& D: What are the trends in logic, memory, analog/mixed signal, 6G, power, packaging, and heterogeneous integration?
2) Advanced Manufacturing: What are the advances and challenges in materials, equipment, and metrology development in the next decade? What EDA and TCAD tools need to be developed?
3) Workforce Development: How do we encourage undergraduates to get interested in semiconductors and nanoelectronics? How do we minimize leakage of the talent pipeline to other industries that use the same skill sets? How do we build up a cadre of technicians in this area using community colleges?
4) Academic Infrastructure: What sort of equipment and at what wafer sizes should NNCI invest in? How are the equipment and staff going to be sustained? What should be the goals of the academic infrastructure?

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Academic Research Challenges for CHIPS Program

DAY 1 SPEAKERS, PANELISTS, AND ORGANIZERS:

SESSION 1 (R&D Challenges)

H.S. Philip Wong
Director of SNF
Stanford
(Session Chair)

Jack Kavalieros
Logic
Intel Fellow

Vijay Narayanan
HI
IBM Fellow

Nirmal Ramaswamy
Advanced/Emerging Memory
VP, Micron Technology

SESSION 2 (Materials, Supplies, & Equipment)

Trevor Thornton
Professor of ECE
Arizona State University
(Session Chair)

Michael Chudzik
Tool Integration
VP, Applied Materials

Victor Moroz
TCAD
Synopsys Fellow

Prith Banerjee
EDA
CTO, ANSYS

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Academic Research Challenges for CHIPS Program

SESSION 3 (Workforce Development)

Shyam Aravamudhan
Director of Core Facilities at JSNN, NCAT
(Session Chair)

Tsu-Jae Liu
Dean and Roy W. Carlson Professor of Engineering
University of California, Berkeley

Gabriela Cruz Thomas
Director of University Research and Collaboration
Intel Corporation

Peter Bermel
Associate Professor
Purdue University

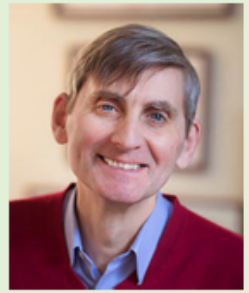
Emmanuel Giannelis
VP for Research and Innovation
Cornell University

Rick McCormick
Principal Scientist
Sandia National Labs

SESSION 4 (Academic Infrastructure)

Sanjay Banerjee
Director of Microelectronics Research Center
Univ. of Texas, Austin
(Session Chair)

Oliver Brand
Executive Director at Georgia Tech
and NNCI Director



Jesús del Alamo
Director of Microsystems Technology Laboratories
MIT

Raj Jammy
Chief Technology Officer
Mitre Engenuity

Larry Goldberg
Senior Advisor
NSF

Jim Plummer
John M Fluke Professor of Electrical Engineering
Stanford

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American Semiconductor Academy: Dean Tsu Jae King-Liu (Berkeley)

A Growing Workforce Development (WFD) Gap

- The U.S. semiconductor industry employs roughly 300,000 workers with technical education and/or training.
  - Over 50% have a college degree and over 25% a graduate degree.
  - 20% only finished high school or do not have a high school diploma.
- U.S. universities/colleges presently do not graduate enough students to meet industry demand for new talent.
  (Additional sources of talent are needed, *i.e.*, via immigration and reskilling.)

- CHIPS Act programs will increase WFD need over the next 6 years, by >3400/yr ***additional*** new college engineering graduates, and >1200/yr ***additional*** new HS/CC technical graduates, on average.

→ Output of U.S. higher-ed. system for the industry should at least double!

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MIT Nano Case Study: Jesus del Alamo

Economics of university fab

Annual fab maintenance + staffing cost ≈ Annual fab fees

Cannot use fab fees to buy new fab tools

" "

Tool suite investment x 0.2 ≈ Annual research volume x 0.2

Annual maintenance and staffing cost: ~20% of tool cost

Research contracts can at most dedicate 20% of budget for fab fees

Tool suite investment ≈ Annual research volume

Economics of university fab vs. wafer diameter

Tool suite investment ≈ Annual research volume

$$\#\text{ Users} \approx \frac{\text{Tool suite investment}}{\$150\text{K}}$$

TOOL SUITE WITH WAFER DIAMETER OF:	COST OF OBTAINING TOOL SUITE (LITHO/DEPOSITION/ ETCHING)	ANNUAL COST OF TOOL MAINTENANCE & STAFFING (20% TOOL COST)	ANNUAL RESEARCH BASE (5X MAINTENANCE & STAFFING COSTS)	#PHD/MASTER'S/ POSTDOCS
150 mm	$15M	$3M	$15M	100
200 mm	$80M	$16M	$80M	533
300 mm	$500M	$100M	$500M	3,333

Inconceivable!

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Workshop Outcomes

- Over 400 registrants
- Satisfaction score: 4.6/5
- Workshop report will be posted on NNCI website

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