MICROELECTRONICS/SEMICONDUCTOR RESEARCH COMMUNITY NSF NNCI WORKSHOP REPORT

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Appendices

- TCAD (Victor Moroz, Fellow Synopsys)
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National Nanotechnology Coordinated Infrastructure

SUMMARY

In response to the recent efforts of the federal government to bolster US semiconductor manufacturing under the auspices of the CHIPS Act, the NSF's National Nanotechnology Coordinated Infrastructure (NNCI) held a two-day virtual workshop to examine how the NNCI can address various components of the CHIPS initiative.

The global semiconductor market is currently over $600B, with an annual growth rate of ~10%, and will drive a $3T electronics market by the end of decade. The US share of this market has fallen to less than 10%, which has clear economic and defense ramifications. This was the impetus for Congress to pass the $52B CHIPS legislation to encourage in-shoring of semiconductor fabs.

The first day of the workshop was devoted to invited talks by industry leaders who discussed the state of the art in their respective fields, and research challenges, highlighting opportunities for academic research. In the morning session, Dr. Kavalieros from Intel focused on advanced transistors for logic applications, Dr. Ramaswamy from Micron discussed advanced memory architectures, and Dr. Narayanan from IBM educated the attendees about heterogeneous integration (HI) as the next paradigm in Moore's law and Dennard scaling. Some of the common themes that emerged are the move toward next-generation 3D devices such as nanosheet transistors, and 2.5D and 3D HI of chiplets of CPU, GPU, high bandwidth DRAMs, and non-volatile memory using hybrid bonding with sub-10 micron pitch for applications such AI/ML using neuromorphic computing. Power management becomes a huge challenge in such 3D systems.

In the afternoon session, Dr. Chudzik from Applied Materials discussed equipment challenges for 300 mm tools which need to handle a wider set of materials, semiconductors beyond Si such as SiC and GaN, and advanced packaging. Dr. Moroz from Synopsys and Dr. Banerjee from Ansys discussed TCAD and EDA challenges, respectively. Moroz pointed out the need for more *ab-initio* simulation methodologies such as density functional theory (DFT) for structure calculations, coupled with non-equilibrium Green's function (NEGF) methodologies for electronic transport, which go beyond the usual drift-diffusion based simulators. Dr. Banerjee pointed out the need to do multi-physics simulations for HI, involving coupled heat and charge transport, as well as high speed simulation of Maxwell's equations to handle parasitics.

The industry overviews on the first day set the stage for sessions on the second day related to workforce development and academic infrastructure. For CHIPS legislation to be impactful, there must be significant renewal of aging academic microelectronics, R&D infrastructure, and a

doubling of graduates in this field to feed into the ecosystem of 300,000 workers in this field in the US. Dr. Liu from Berkeley talked about the proposed American Semiconductor Academy which would marshal the resources of universities and community colleges to fill the pipeline for college graduates and technicians needed by industry, and provide them with the multi-disciplinary training in device physics, materials science, circuits, and architectures to perform device technology co-optimization (DTCO) and system technology co-optimization (STCO) that will be increasingly needed in the future. Intel provided an industry perspective of future workforce needs. Case studies of what academia has started doing in this area were discussed by Purdue and Cornell.

A key question that this workshop attempted to answer was how to revamp the aging academic cleanrooms. For example, what wafer size should universities target in the future, and how would these more expensive facilities be maintained? Dr. Del Alamo from MIT discussed a "business model" for new academic facilities and suggested that 200 mm (CMOS + X) may be the "sweet spot" for academia. State-of-the-art 300 mm tools would be prohibitively expensive to maintain, while tools handling wafer sizes smaller than 200 mm may not be supported by the equipment manufacturers. However, to sustain these academic cleanrooms, the university needs to have an annual research portfolio comparable to the infrastructure investment, which may limit the number of such facilities that the US can justify. A slightly contrarian view was expressed by Dr. Plummer from Stanford who felt that universities should focus on TRL-1 type exploratory research and not invest in expensive 200 mm CMOS capabilities. Dr. Brand from Georgia Tech and Dr. Goldberg from NSF discussed the NSF National Nanofabrication Coordinated Infrastructure (NNCI), which sponsored this workshop. NNCI is a geographically diverse network of sixteen universities and partners in the US which provides cleanroom access to internal and external academic and industrial users. It may make sense to use CHIPS funding to build on the extremely successful NNCI model to expand the capabilities and geographical reach of NNCI.

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1: INTRODUCTION

The NSF'S NNCI program supports a geographically distributed network of open-access microelectronics and nanotechnology cleanroom and characterization user facilities across the US. The NNCI held an online workshop on September 8 and 9, 2022 in response to the federal government's recent initiatives to strengthen domestic semiconductor manufacturing. The goal of the workshop was to generate a white paper that could inform CHIPS funding as it relates to USICA, NSTC, NAMP, the Microelectronics Commons, NSF Engines, and FuSe.

The workshop combined invited talks by leading academic, industry, and government researchers with panel discussions and it was organized into four sessions that included the following topics and issues:

1) **Semiconductor R & D Challenges:** What are the trends in logic, memory, analog/mixed signal, 6G, power, packaging, and heterogeneous integration
2) **Advanced Manufacturing (Materials, Supplies & Equipment):** What are the advances and challenges in materials, equipment, and metrology development in the next decade? What EDA and TCAD tools need to be developed?
3) **Workforce Development:** How do we encourage undergraduates to get interested in semiconductors and nanoelectronics? How do we minimize leakage of the talent pipeline to other industries that use the same skill sets? How do we build up a cadre of technicians in this area using community colleges?
4) **Academic Infrastructure:** What sort of equipment and at what wafer sizes should NNCI invest in? How are the equipment and staff going to be sustained? What should be the goals of the academic infrastructure?

2: RESEARCH & DEVELOPMENT CHALLENGES

Dr. Kavalieros from Intel focused on advanced transistors for logic applications, Dr. Ramaswamy from Micron discussed advanced memory architectures, and Dr. Narayanan from IBM educated the attendees about heterogeneous integration as the next paradigm in Moore's law and Dennard scaling. Some of the common themes that emerged are the move toward next-generation 3D devices such as nanosheet transistors, and 2.5D and 3D heterogeneous integration (HI) of chiplets of CPU, GPU, high bandwidth DRAMs, and non-volatile memory using hybrid bonding with sub-10 micron pitch for applications such artificial intelligence/machine learning (AI/ML) using neuromorphic computing. Power management is a huge challenge in such 3D systems.

2.1: Advanced Transistors for Logic, Jack Kavalieros (Intel Fellow)

MOSFET scaling for logic has evolved from planar Si devices based on silicon dioxide gate dielectric and polysilicon gates to metal gate, high-k (MGHK) and enhanced mobility channel materials based on strain engineering, followed by a shift to 3D devices based on FinFETs. More recently, there has been a shift to more complex 3D architectures based on nanosheet channels created from growth of Si/SiGe multilayers, and selective etching of the sacrificial SiGe layers. Multi-V_T FETs have been achieved using gate metal work function engineering. For back end of the line (BEOL), advances have included moving away from Cu based dual damascene and low-k dielectrics to subtractive interconnect technologies based on non-Cu metallization such as Ru or topological interconnects, and separating signal lines on the front of the chip to buried power rails on the back side.

2.2: Memory Architectures, Nirmal Ramaswamy (VP, Micron)

Globally, 2.5 quintillion or exabytes of data are generated daily with an annual growth rate of 23%, driven by big data applications such as AI/machine learning and autonomous driving. DRAM cells have evolved from planar access transistors and storage capacitors to recessed access devices, 3D MIM or MIS storage capacitors, and close packed hexagonal cell layouts. Taking the lead from 3D NAND architectures, the next generation of DRAMs will have 3D stacked cells. Key challenges that academia might address include reliability issues such as variable charge retention times in cells, row hammer and cell disturbs in these compact 3D cells. NAND has long moved to 3D stacks, and Micron currently can make a 1Tb, 232-layer NAND memory using polysilicon channels. Academic research opportunities exist in alternative channel materials which can provide higher NAND string currents. There is a heterogeneity of types of data (hot, warm, and cold) and storage types (DRAM, NVM, novel memory such as RRAMs, STT and PCM).

2.3: Heterogeneous Integration, Vijay Narayanan (IBM Fellow)

Heterogeneous integration (HI) of disaggregated chiplets in 2.5D and 3D using hybrid bonding and Si interposers is going to be increasingly important because Moore's law scaling of planar ICs is facing limits in terms of Power, Performance Area/Cost (PPAC) metrics. This will create new challenges in the 100 W/cm^2 "power wall" which has limited chip frequencies to 3GHz for the last decade. In addition to digital logic using von Neumann architectures, there will be increasing effort in neuromorphic computing for AI/ML using analog approaches. These may be based on Long- and Short-Term Memory (LSTM) using RRAMs or PCMs for training the neural Multiply and Accumulate (MAC) architectures.

3: MATERIALS, SUPPLIES, & EQUIPMENT

Mike Chudzik from AMAT emphasized the tool and process challenges with the introduction of new semiconductor materials, gate-all-around transistors and advanced packaging approaches. Victor Moroz from Synopsis discussed transistor and interconnect evolutions, along with an industry logic roadmap, including DTCO and STCO. Prith Banerjee from Ansys discussed multiscale, multidomain, and multiphysics simulations for 3D IC, chip package, and semiconductor manufacturing.

3.1: Tool and Process Challenges for Advanced Systems, Mike Chudzik (VP, AMAT)

There are significant material challenges in logic, memory, and integration, as also discussed in the session on R&D challenges. For example, device and materials inflections in logic and discrete devices will impact tooling process requirements. The introduction of new semiconductor materials and advanced packaging for advanced systems will drive the scaling of package wiring dimensions for bump bonding, die to wafer bonding, and wafer to wafer hybrid bonding in mass production. The industry's future will be heavily influenced by the third generation of semiconductors (SiC, GaN, etc.) for EVs and consumer devices, not just as standalone discrete devices, but also as integrated devices at the package level. With the promise of the gate-all-around era, the industry can expect a lot of scaling in the next decade. However, there are many challenges at the tool and process level, including metal gate in nanosheets, multi work function materials inside and in between nanosheets, inter spacer to reduce overlap capacitance, selectivity, material substitution, etching challenges, and characterization challenges etc. The co-integration of new semiconductor materials on a package will require a higher density of devices to take advantage of higher performance and higher bandwidth. The highest pitch is going to drive the technology, with wafer-to-wafer hybrid bonding. Real world examples of advanced packages in Intel logic and in Apple devices were presented.

3.2: Modeling in Advanced CMOS Logic, Victor Moroz (Synopsys Fellow)

Short-term (1-2 years) and mid-term (up to 5 years) industry research typically is highly secretive, which is problematic for collaborations with academia. At a minimum, academia should be able to engage with industry and contribute towards mid-term research goals, such as materials engineering, technology design, etc.

The latest research indicates that 2D materials can get to 1-4 nm nodes, but these small process sizes have a lot of technology issues such as defects and imperfections, etc. An idealized 2D material CFET (no defects, or traps) is 2X behind Si CFET in ring oscillator benchmarking tests. In a MOSFET configuration, 2D materials are not ideal either. So, even though Si has some

fundamental limitations, it is here to stay for at least 10 years. The expected transistor evolution going forward likely will be GAA to CFET to 3D Si stacking. Next, interconnect resistance increases sharply beyond the 3 nm node, with cobalt only improving it marginally. Pitch scaling is forecasted to slow down around 20 nm. Ab-Initio material engineering will explore electron scattering at grain boundaries in narrow wires, and with variable grains, compositions, etc. In porous dielectrics, electric permittivity (which decreases capacitance) versus mechanical strength will be studied and optimized. The industry logic roadmap shows design technology co-optimization (DTCO) scaling (beyond the 3 nm node) rather than lithography scaling. DTCO is the main vehicle for transistor density scaling and will keep Moore's law going through 2030. Lastly, system technology co-optimization (STCO), 3D IC stacking, and 3D place, and route are necessary to go beyond 2D IC limits and will provide a breakthrough beyond 2030. This will require fundamental changes in the IC design paradigm.

3.3: Future of Simulation Driven Innovation in Nanotechnology Research, Prith Banerjee (Ansys CTO)

Generational drivers of simulations include autonomous vehicles, 5G, hyperscale computing, AI/ML, and IIOT. Simulation is an increasingly powerful tool for performing multi-physics simulations, modelling interactions between semiconductors, and studying mechanical, electromagnetic, and fluidic properties. As technology nodes scale from FinFETs, GAA, and nanosheets to CFETs and chiplets, key challenges may arise in front side vs back side power/power integrity, thermal/mechanical, electromagnetics/signal integrity, interconnects etc. Modeling could be the way to address these complex problems. For instance, modeling photonics and semiconductor chips in the same package, could elucidate the power reduction and increased speed that is observed for these co-packaged entities. Three areas for simulations – (1) 3D IC simulation solutions (e.g., soft IP optimization and chiplet verification); (2) chip package system (e.g., multiscale, multidomain, and multiphysics simulation from the chip to the system to address power and signal integrity, ESD, EMI/EMC, and thermal/mechanical integrity); (3) semiconductor manufacturing (e.g., fab processes, poly Si and crystal growth). In summary, the EDA industry has solved design complexity for digital systems by high level synthesis, RTL synthesis, physical synthesis, and verification at each level (system, RTL, gate, physical), but it is a hard challenge for analog systems. A grand challenge is how best to leverage AI/ML, HPC, and cloud in EDA synthesis, verification, and validation methods for complex systems.

4: WORKFORCE DEVELOPMENT

Dr. Tsu-Jae King Liu, Dean of Engineering at UC Berkeley, and Dr. Sowmya Venkataramani, University Program Director at Intel Labs, described recent initiatives and investments in workforce development from academic and industrial perspectives. Dr. King-Liu outlined progress in establishing the American Semiconductor Academy (ASA), a nationwide semiconductor education and training network of universities and colleges. Dr. Venkataramani described Intel's university research programs and the recent $50M investment at Ohio State University. A group of panelists discussed issues facing workforce development programs. It will be important to develop both human and infrastructure capacity at 4-year schools and community colleges to meet the demand for a well-trained semiconductor workforce.

4.1: Introduction to the ASA Initiative, Tsu-Jae King Liu (Dean of Eng., Berkeley)

Despite the ubiquity of semiconductor systems in our daily lives, the broader microelectronics industry is largely invisible to the US public. This is despite that fact that 49 states have companies working in semiconductors or a related field. For this reason, jobs in the semiconductor manufacturing industry are perhaps not as attractive to college students as those in software, artificial intelligence, and machine learning. The recently passed CHIPS and Science Act will increase workforce development needs over the next six years by >3,400 new college graduates and >1,200 new high school and community college technical graduates. The vision for the American Semiconductor Academy (ASA) initiative is to secure America's global leadership in semiconductor manufacturing in part by attracting students into semiconductor-related fields of study. The ASA is partnering with SEMI Corporation to ensure that academia addresses industry needs by revitalizing the microelectronics curriculum, providing facilities for hands-on training, and diversifying the talent pathway.

4.2: Shaping the Future – Intel's Academic Collaborations, Sowmya Venkataramani (University Program Director, Intel Labs)

Intel has >121,000 employees in 53 countries including more than 6,500 in the 'semiconductor heartland' of Arizona, New Mexico, and Ohio. These jobs require technicians, engineers and scientists with associates, bachelors, and graduate degrees from many STEM disciplines. Intel's academic outreach mechanisms include large center activities in partnership with the Semiconductor Research Corporation and the National Science Foundation; mid-size centers and individual research grants; and the Mindshare program for campus recruiting with the goal of diversifying the higher education talent pool. The first phase of a $50M investment in the Intel Semiconductor Education and Research Program for Ohio will fund proposals from universities and community colleges in the state to develop semiconductor-focused education and workforce programs.

4.3: Panel Discussion: Peter Bermel* (Purdue), Emmanuel Giannelis* (Cornell), Rick McCormick (Sandia)

All three panelists highlighted the need for educational initiatives that strengthen technician training and associate degree programs at community colleges. These include developing certificate programs aligned with existing associate degree curricula and offering hands-on activities such as internships and research experiences for undergraduates and teachers from local community colleges. There is a need for industry-standard tools in teaching cleanrooms, as opposed to research tools that are more common in R&D facilities. But these tools are expensive to acquire and maintain and will require on-going support from industry after initial funding from e.g., the NSF ATE program expires. Continuing challenges are the need to recruit US students for jobs at National Labs and increasing the number of H1B visas available each year.

5: ACADEMIC INFRASTRUCTURE

Dr. Oliver Brand, Director of the NNCI coordinating office, and Dr. Jesus del Alamo, Director of the Microsystems and Technology Labs at MIT, discussed the current state of microelectronics and semiconductor academic infrastructure and the needs for the future. Dr. Brand presented an overview of the NNCI network and the educational opportunities it provides, emphasizing the invaluable asset of staff expertise. Dr. del Alamo described a business model for academic cleanrooms that concluded 200 mm tools would be educationally impactful while still being financially practical. In a panel discussion, the value of investing in 200 mm capable cleanroom infrastructure versus tools geared towards exploratory research was debated.

5.1: Overview of NNCI, Oliver Brand (NNCI)

40-plus years of NSF-funded nanofabrication infrastructure has established a well-connected network of university facilities around the nation. Today, there are 16 NNCI sites and 13 partners in 16 states, with a total of 71 facilities and over 2,200 tools. This extensive network provides open access to state-of-the- art nanofabrication and characterization facilities and their tools across the US, as well as staff expertise. These resources not only support research, but they also are a valuable resource for education and outreach and studies of societal and ethical implications in and of nanotechnology. The network approach makes the whole more than the sum of its parts.

The micro-and nano-scale fabrication and characterization facilities cover research and education in nanomaterials, electronics, photonics and optics, NEMS/NEMS, basic science such as chemistry and physics, as well as medicine and life sciences and geology and earth sciences. It also includes computation and modeling capabilities. Nanofabrication techniques include top-down (lithography defined) as well as bottom-up (synthesis-based) techniques.

About one-third of publications referencing NNCI awards contain the search term “semiconductor.” As such, “semiconductors” and microelectronics research constitute by far one of the most important research and education areas of the NNCI. In addition to academic users, NNCI facilities are heavily used by start-ups as well as small and large companies.

A key attribute of academic nanofabrication infrastructure is that it is flexible and low-cost. An often overlooked attribute is the staff expertise. The staff expertise is an essential resource for process knowledge and enables newcomers to get started right away in the shortest amount of time. The NNCI is ideal for trying out new ideas using new materials, devices, and process modules.

Because of the long history of NNCI and some of the academic facilities, many of the clean room infrastructures are beginning to show signs of aging. Many tools are more than 10 – 20 years old

and some of them are not supported by the vendor anymore, let alone keeping up with the industry standard. Universities are not set up to constantly refresh capital investments (as most industrial companies are, using a depreciation schedule). Most academic facilities have limited capabilities for 200-mm tools and beyond. There is a strong need to invest into upgrading toolsets not only to have the most advanced capabilities, but also even to keep workhorse process capabilities available with stable operation.

Because of the need to support research on new ideas and concepts, it is not feasible to have "standard" processes. As such, there is limited capability to support translational (lab-to-fab translation) activities that require stable, highly reproducible processes. This is not a failure of the academic facilities; rather, it is the intrinsic nature of facilities for which the mission is to discover and to invent.

To bridge the lab-to-fab gap, this nation needs to augment the university facilities with additional tools (that provide "standard processes") and staff that will keep the process stable and reproducible.

5.2: Reasserting US Leadership and Role of Universities, Jesus del Alamo (MIT)

A case study of one of the most advanced academic cleanrooms recently commissioned at MIT was also discussed by Dr. del Alamo from MIT. He described a "business model" for new academic facilities and suggested that 200 mm (CMOS + X) may be the "sweet spot" for academia. State-of-the-art 300 mm tools would be prohibitively expensive to maintain, while tools handling wafer sizes smaller than 200 mm may not be supported by the equipment manufacturers. However, to sustain these academic cleanrooms, the university needs to have an annual research portfolio comparable to the infrastructure investment, which may limit the number of such facilities that the US can justify.

5.3: Panel Discussion: Raj Jammy* (Mitre), Larry Goldberg (NSF), Jim Plummer (Stanford)

Dr. Goldberg from NSF provided a historical context of the NNCI program, as well as the precursor programs that date back to 1995. A slightly contrarian view to Prof. del Alamo was expressed by Dr. Plummer from Stanford who felt that universities should focus on TRL-1 type exploratory research and not invest in expensive 200 mm CMOS capabilities.

6: CONCLUSIONS / FUTURE DIRECTIONS

A key question that this workshop attempted to answer was how to revamp the aging academic cleanrooms. For example, what wafer size should universities target in the future, and how would these more expensive facilities be maintained? It may make sense to use CHIPS funding to build on the extremely successful NNCI model to expand the capabilities and geographical reach of NNCI. It was concluded that academic cleanrooms should not invest in 12-inch capability because of the expense of the equipment and operating costs. 8” may be the “sweet spot” where leading edge tools can be acquired and maintained at a sustainable cost. However, smaller wafer sizes such as 6” may also be a viable option for TRL 1 level work done by universities.

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NSF CHIPS Act Workshop: Materials, Supplies, & Equipment

Victor Moroz, Synopsys Fellow

September 8, 2022

Outline

- **Transistor evolution**
- **Interconnect evolution**
- **Ab-Initio material engineering**
- **Industry logic roadmap**
- **DTCO + STCO**
- **Summary**

Outline

- **Transistor evolution**
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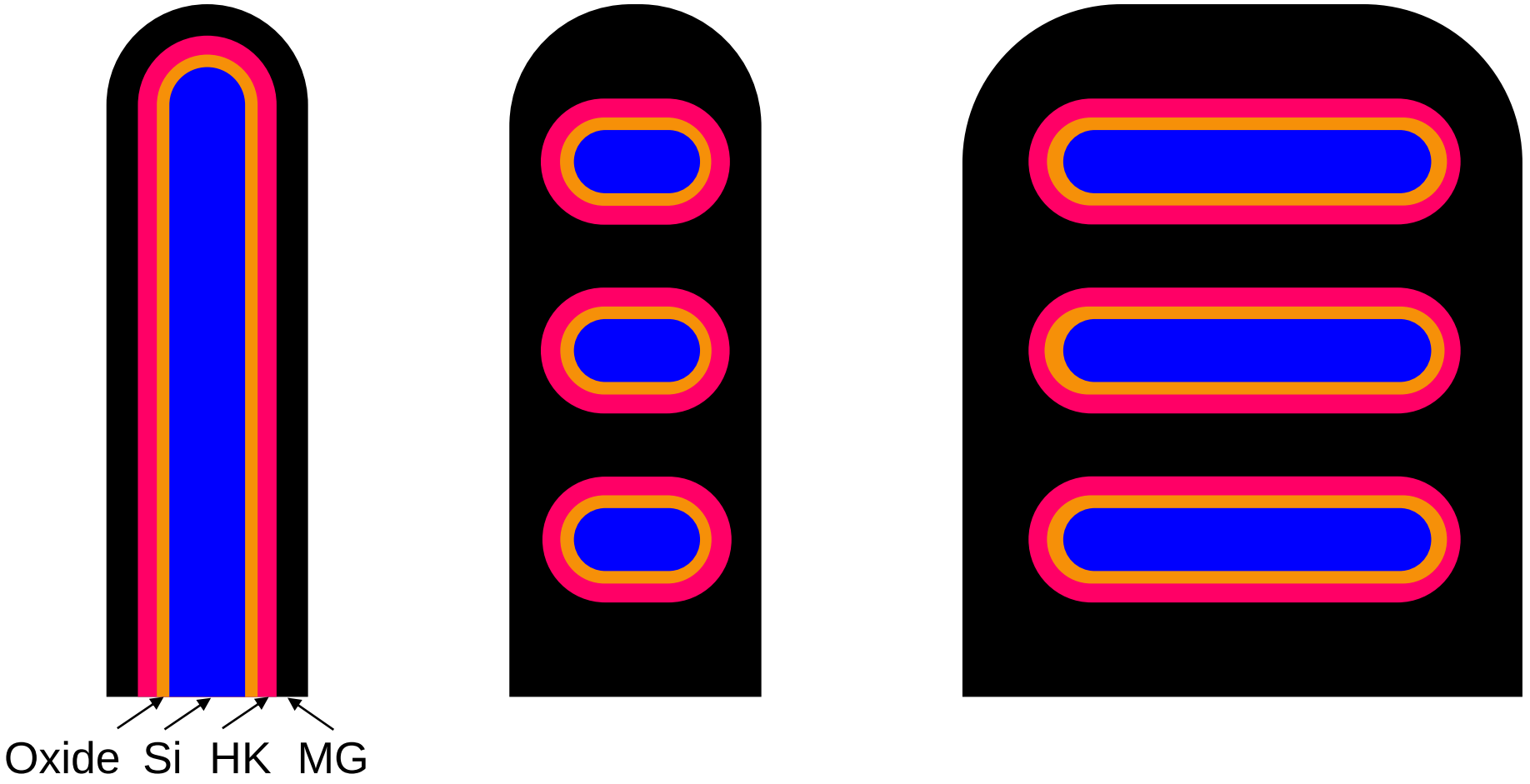
Typical FinFET and GAA Transistors

Logic FinFET

SRAM GAA (narrow)

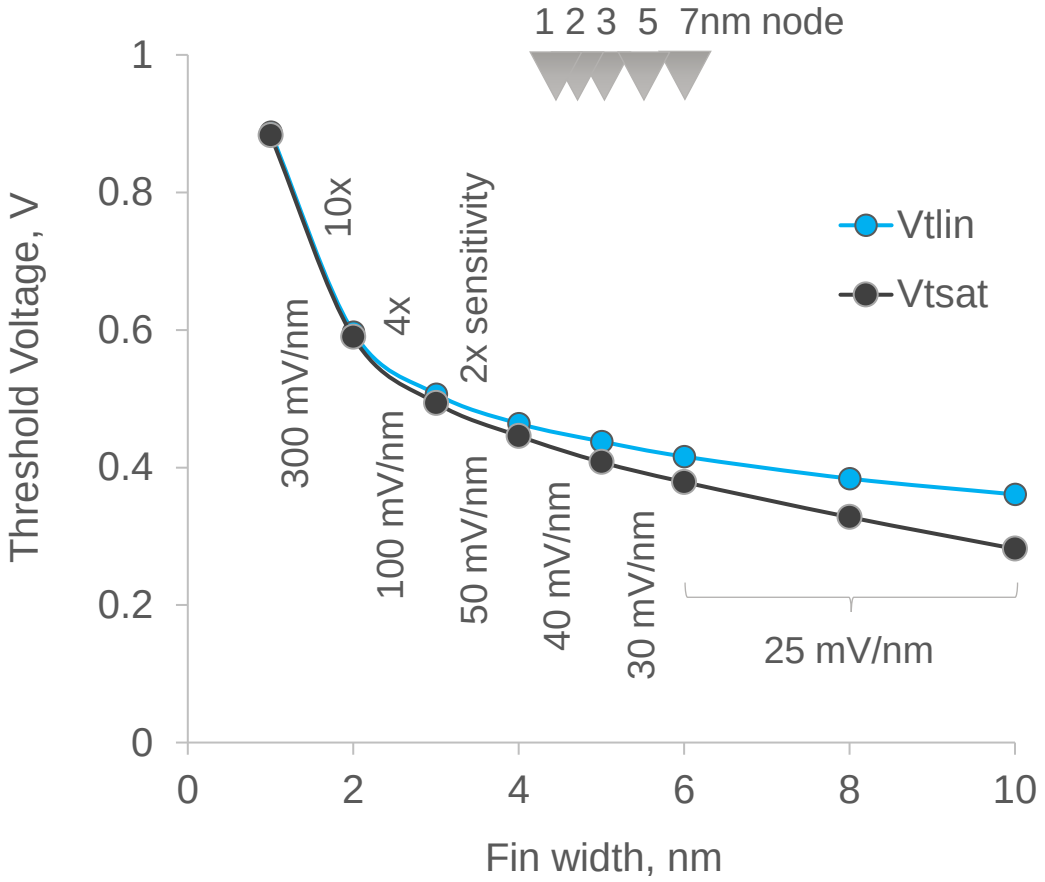
Logic GAA (wide)



Channel sizes for GAA are similar to the FinFET

These sketches show channel cross-sections, with the current flowing into the screen

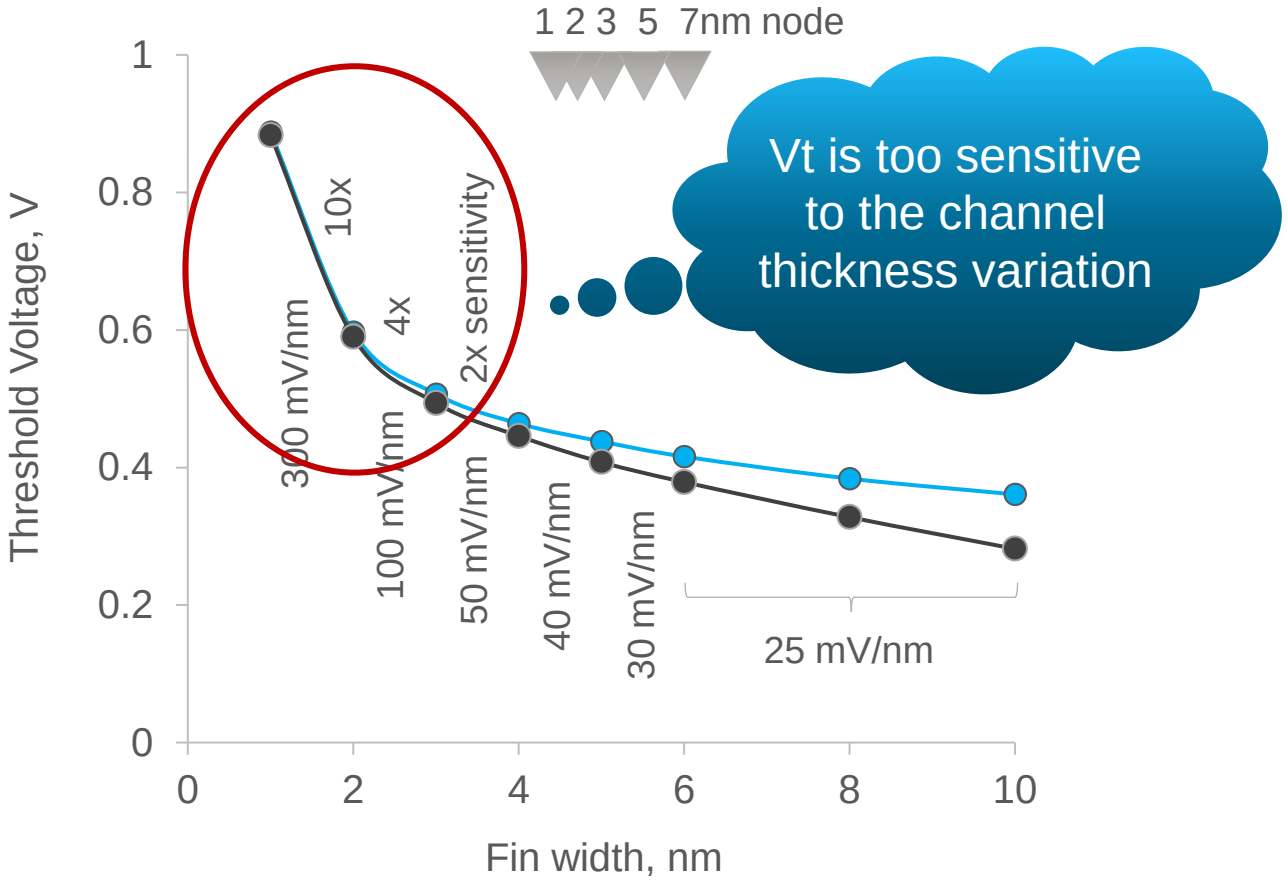
NEGF Quantum Transport: Vt Sensitivity to Fin Width



L = 15nm
Fixed gate workfunction
Undoped channel
NEGF with phonon and surface roughness scattering

- Vt is increasing with fin width scaling due to the band gap widening
- Fin patterning has to be done with spacer assisted patterning

NEGF Quantum Transport: Vt Sensitivity to Fin Width



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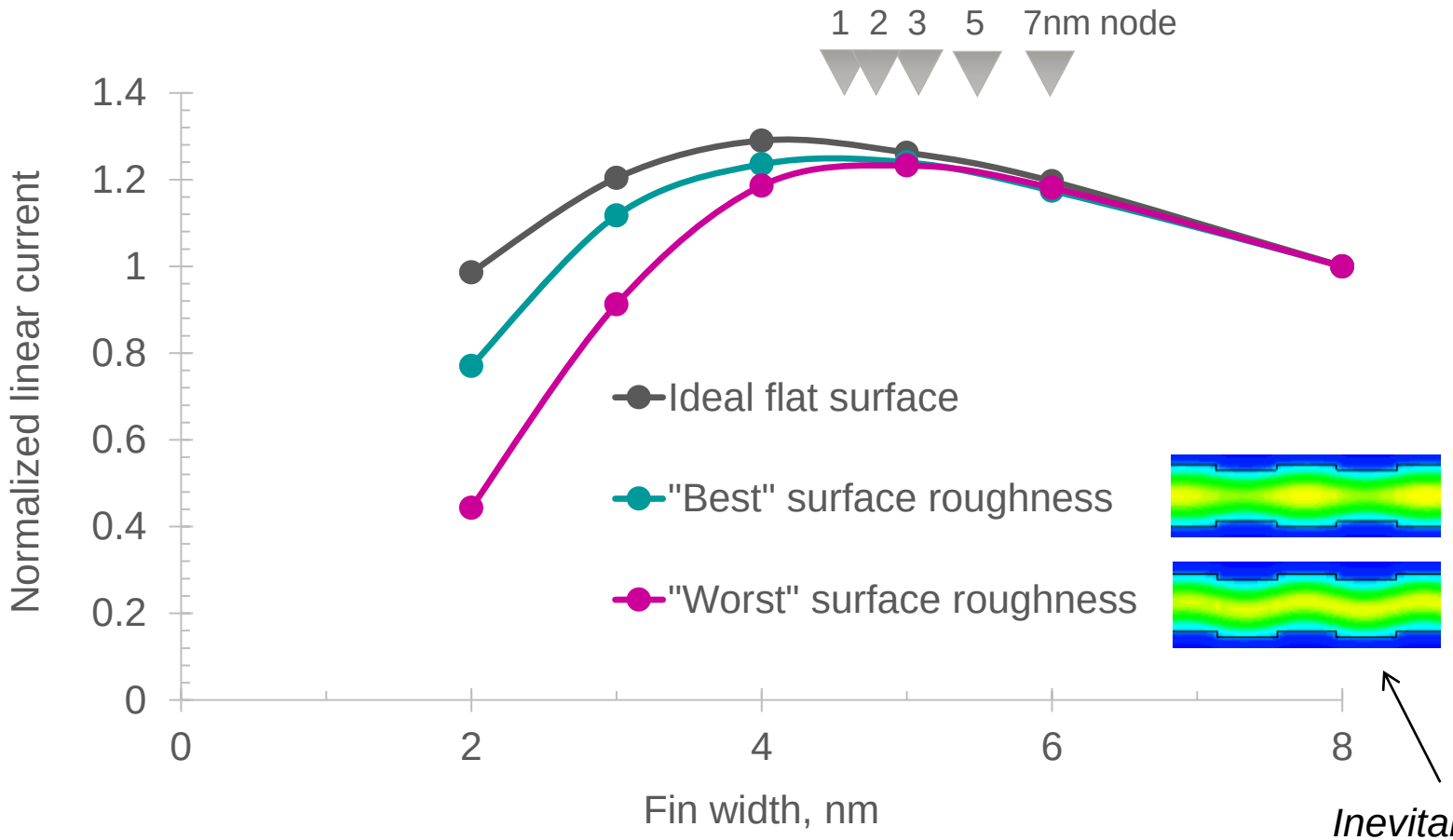
Quantum Transport Model: Driving Strength vs Fin Width

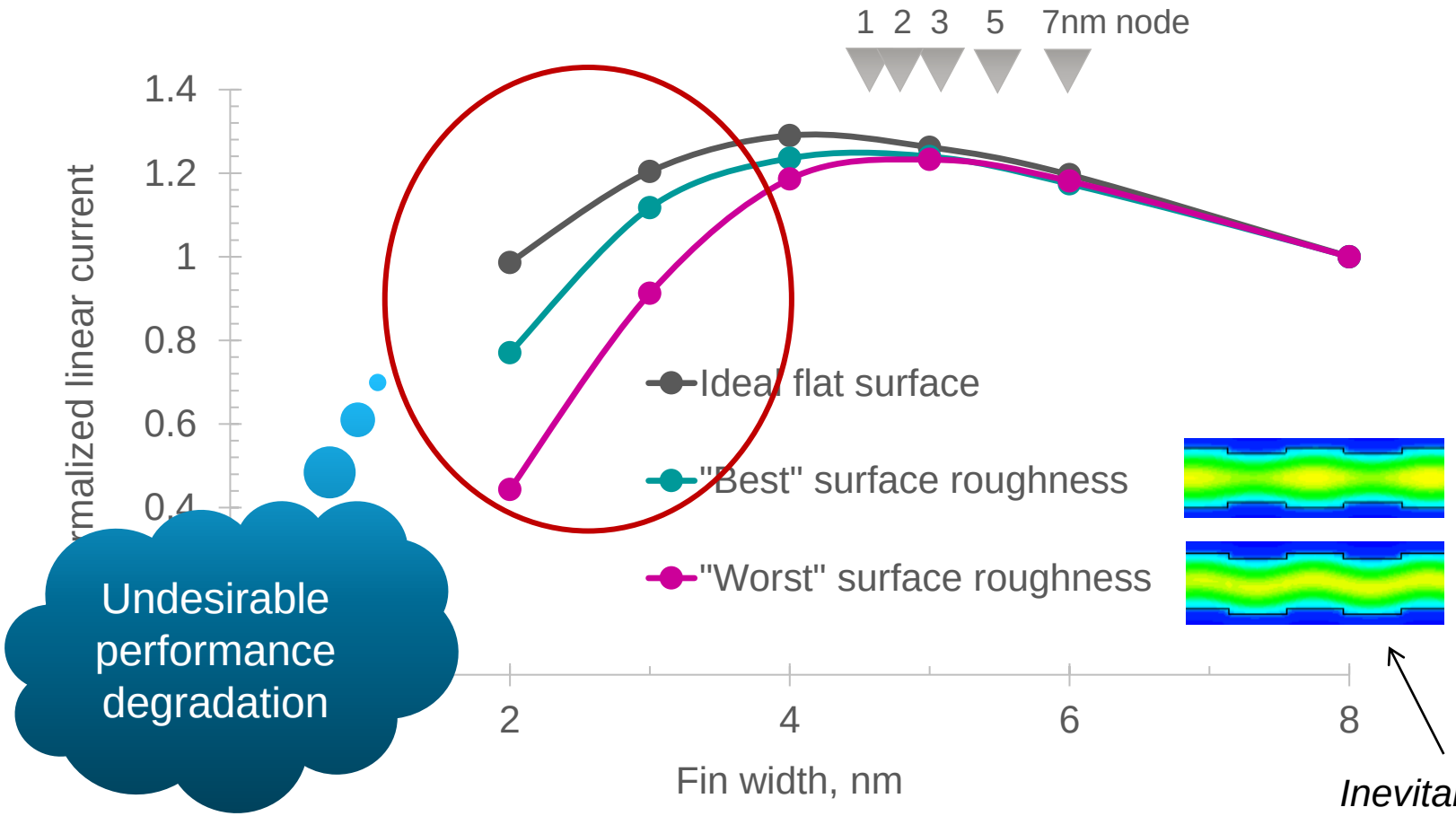


Inevitable 1 mono-layer interface steps

- You don't want to go below 4 nm fin width because of:
  - Performance degradation
  - Performance variability
- No drastic performance loss down to ~1 nm design rules

L = 15 nm
Ioff = 1 nA/um by adjusting gate workfunction
Undoped channel
NEGF with phonon and surface roughness scattering

Quantum Transport Model: Driving Strength vs Fin Width



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Inevitable 1 mono-layer interface steps

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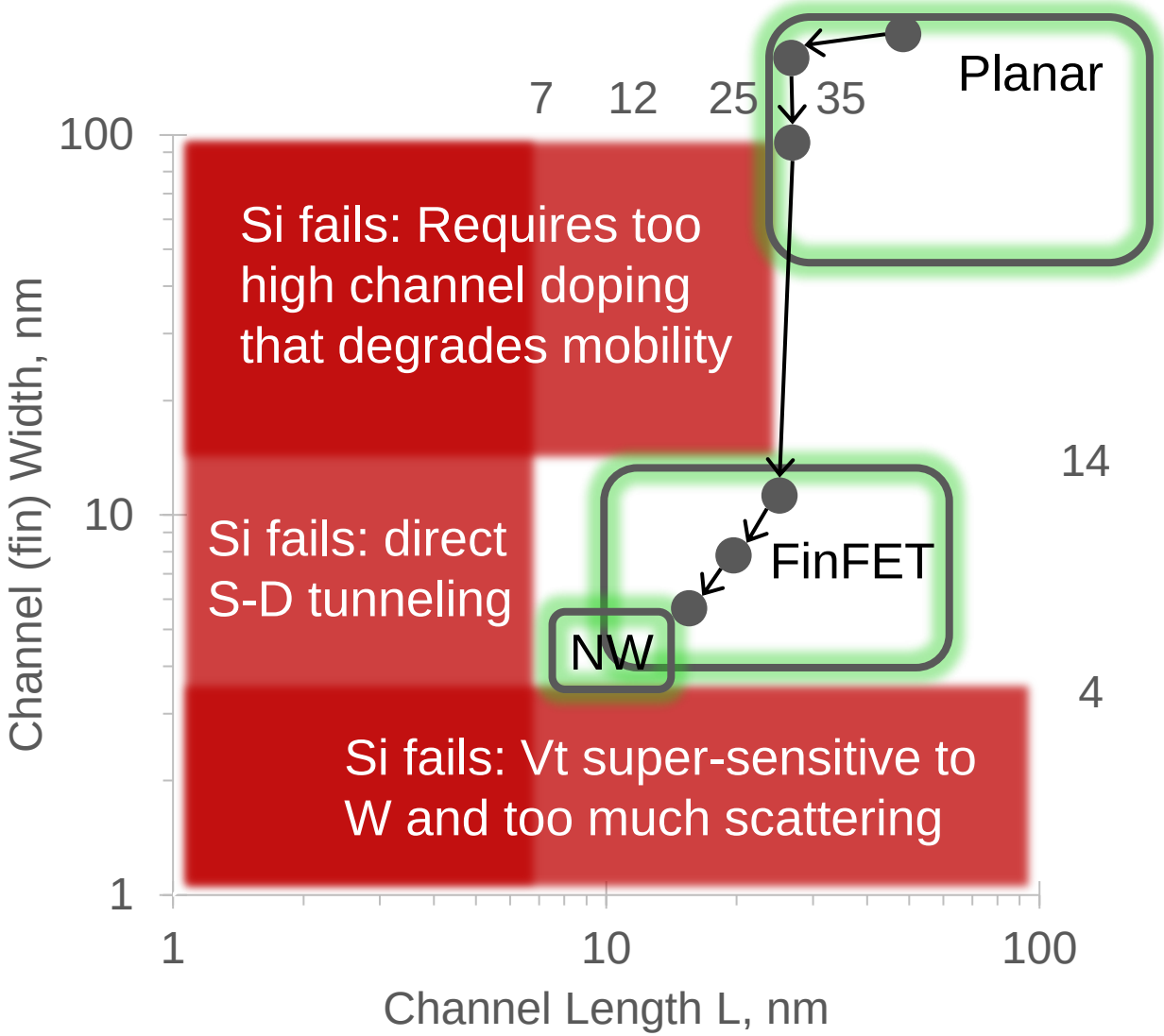
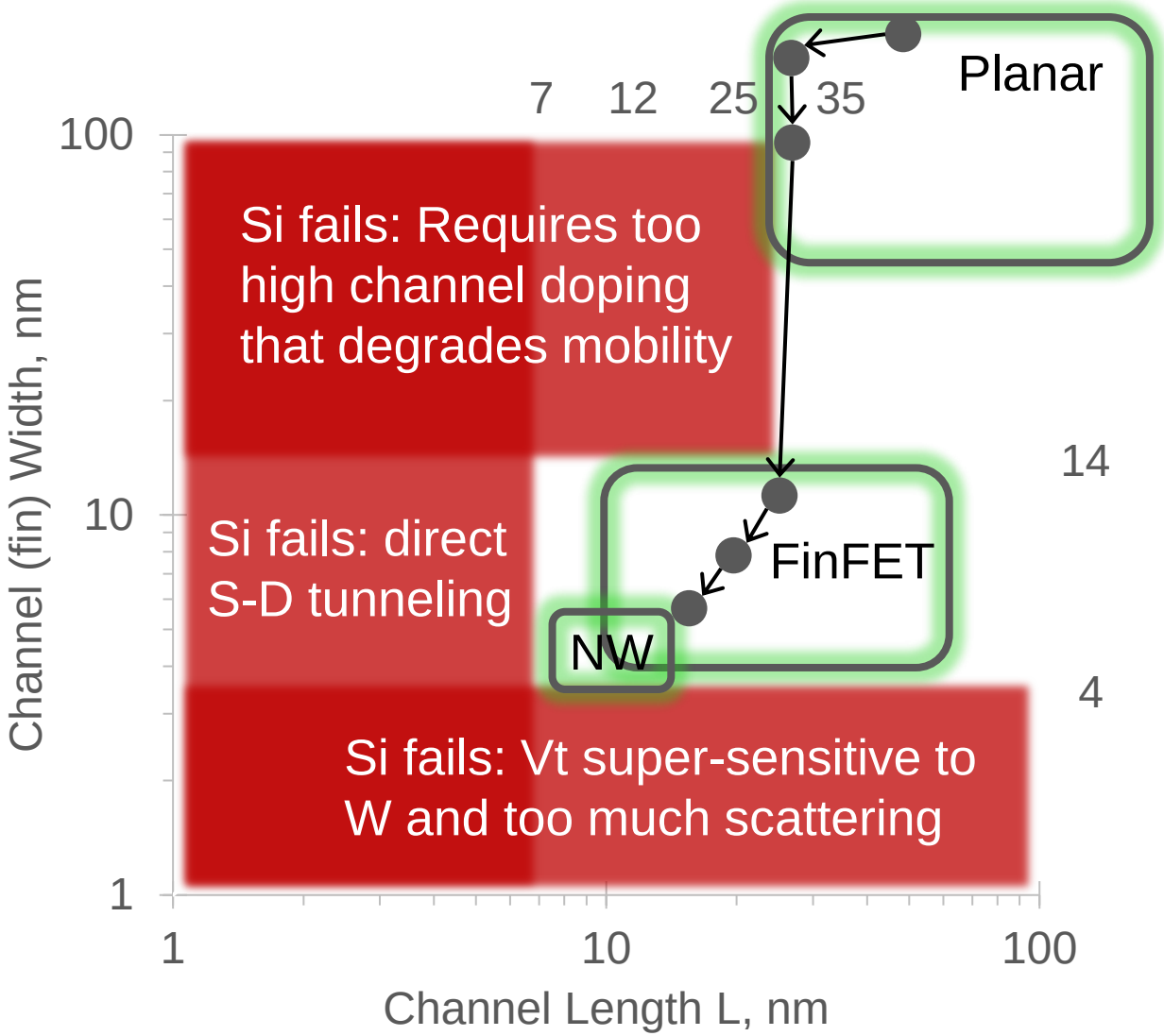
Transistor Architecture Landscape



- Transistors are designed around fundamental limitations

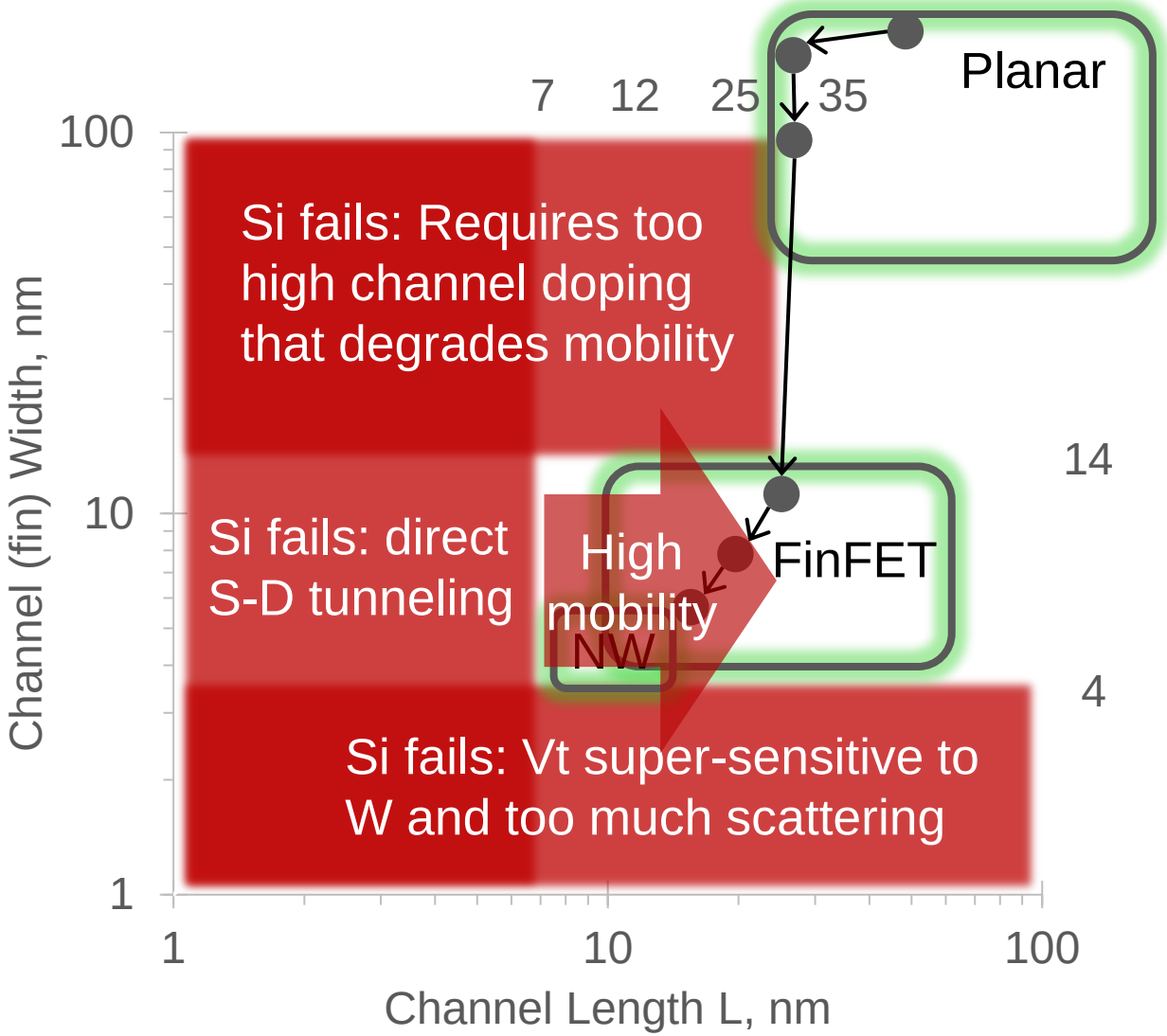
Transistor Architecture Landscape



- Transistors are designed around fundamental limitations

We are stuck in the corner here, so no more transistor scaling is expected

Transistor Architecture Landscape

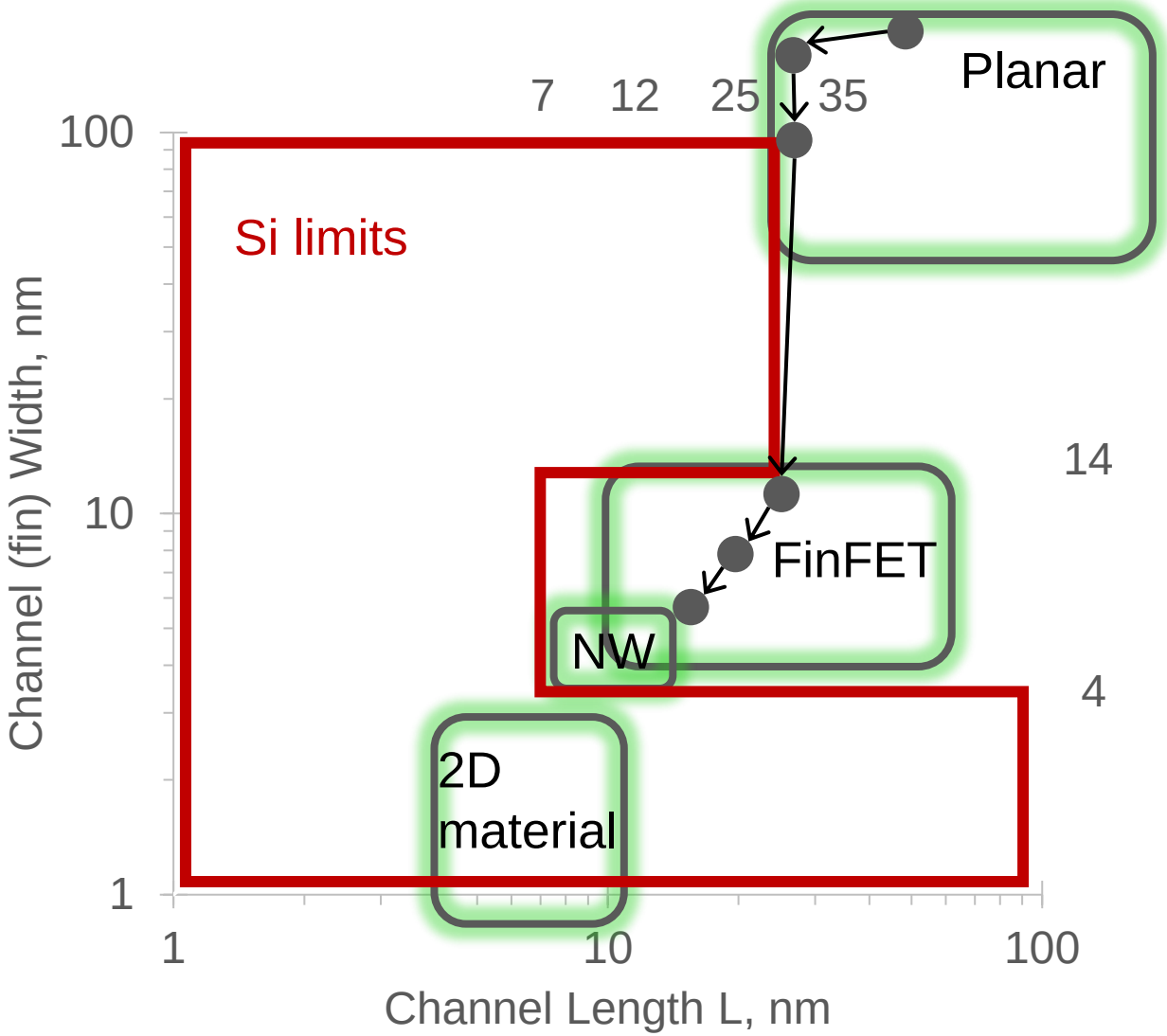


- Transistors are designed around fundamental limitations

We are stuck in the corner here, so no more transistor scaling is expected

High mobility channel scales even worse than Si, so it's time to move to low mobility channels!

Transistors Beyond Silicon

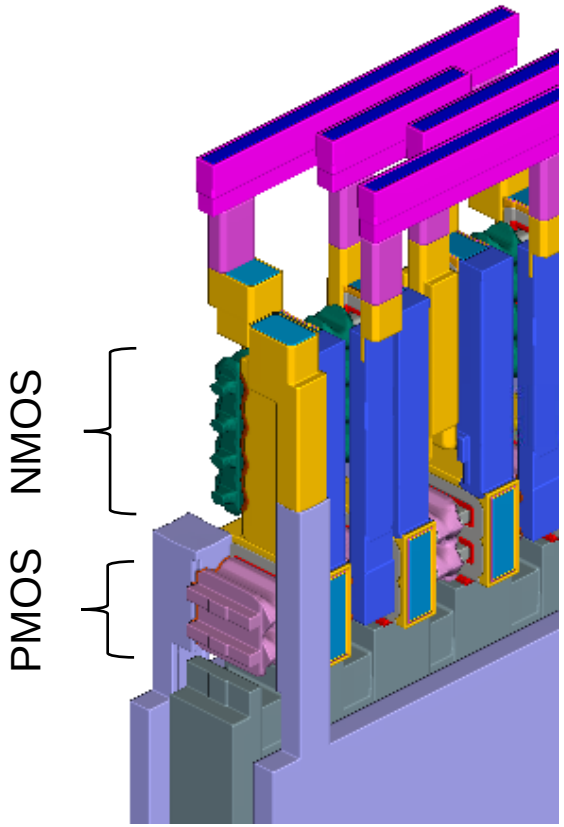


2D material can shave off a couple on nm, but they are behind Si in driving strength…

2D Material MOSFET is Not Competitive

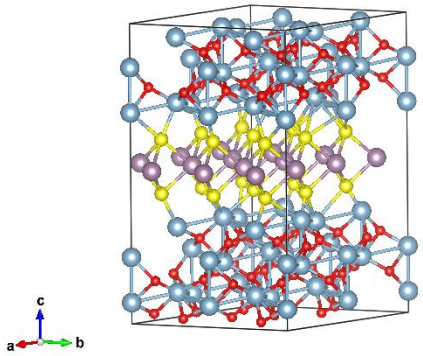
Even idealized WS2 CFET (Ohmic contacts and no interface traps) is far behind Si

Silicon CFET

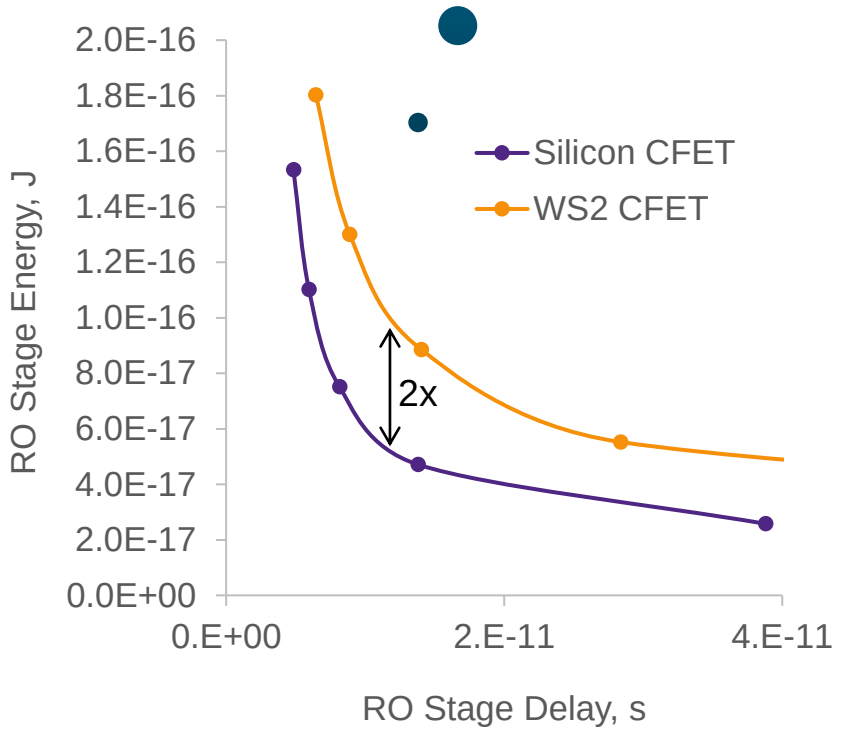


2D Material CFET

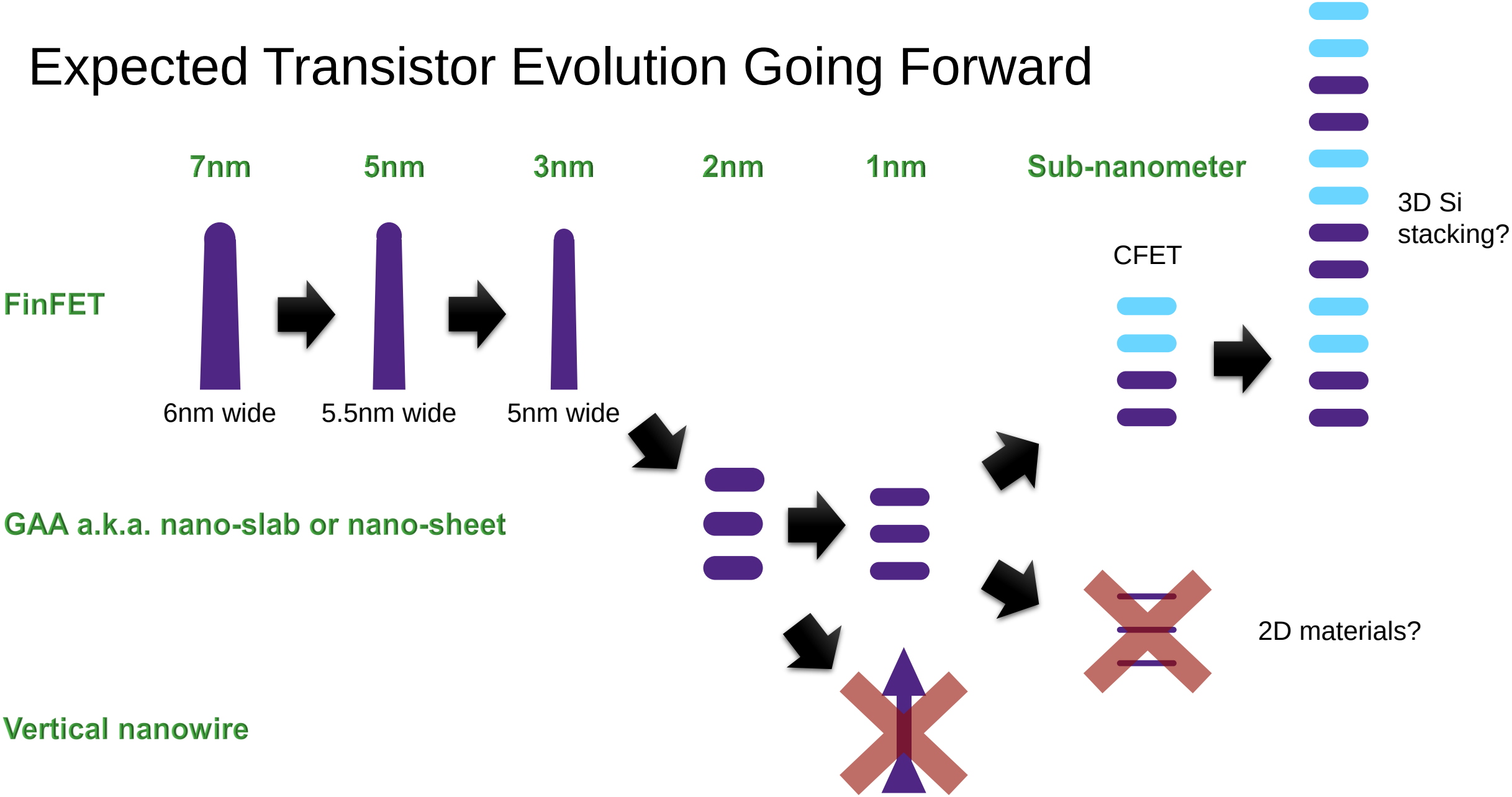
- Each Si channel is replaced by 2 WS2 channels
- Quantum transport analysis with and w/o defects/imperfections



Ring Oscillator Benchmark



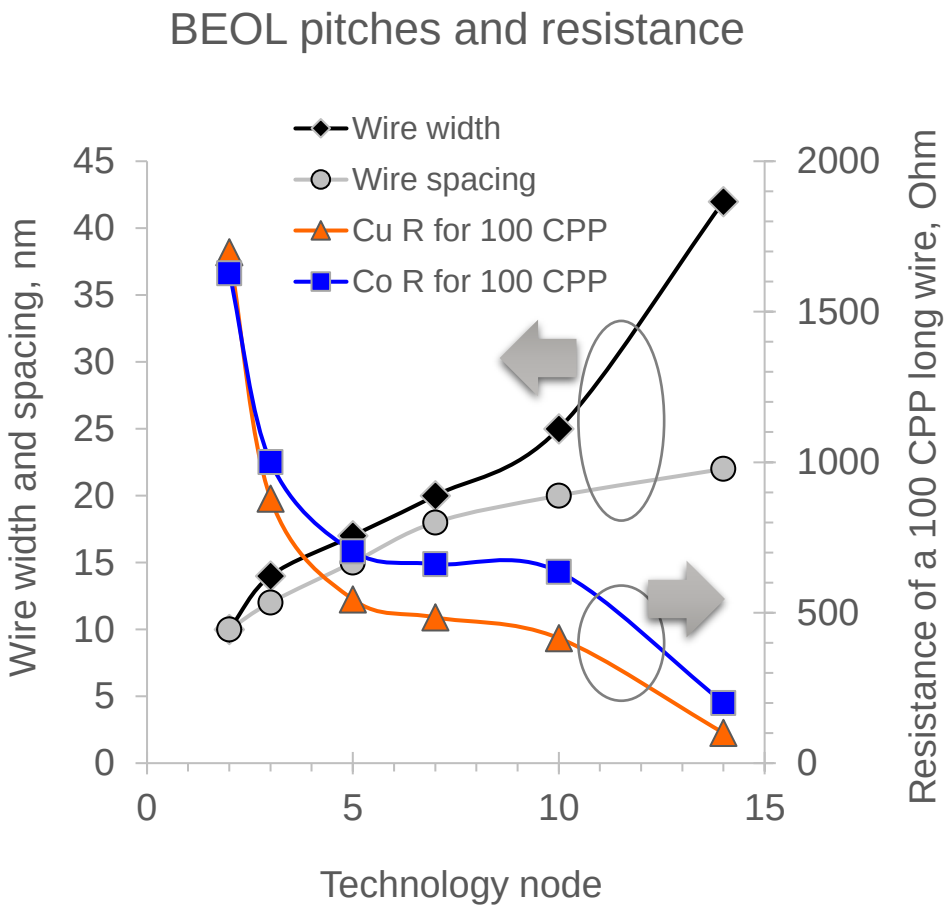
Expected Transistor Evolution Going Forward



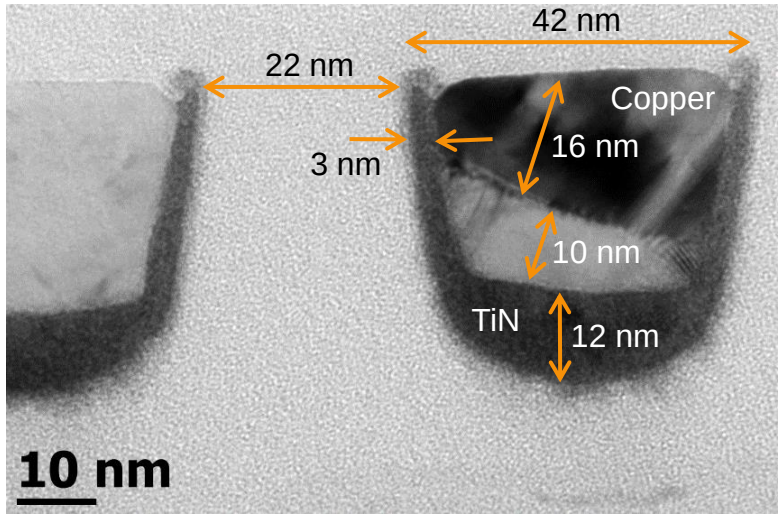
Outline

- Transistor evolution
- **Interconnect evolution**
- Ab-Initio material engineering
- Industry logic roadmap
- DTCO + STCO
- Summary

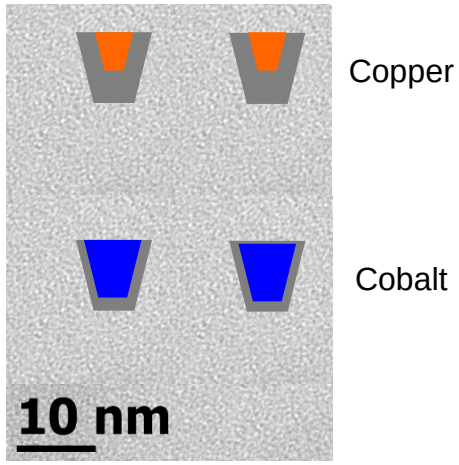
Interconnect Resistance Evolution



14nm node:



2nm node:



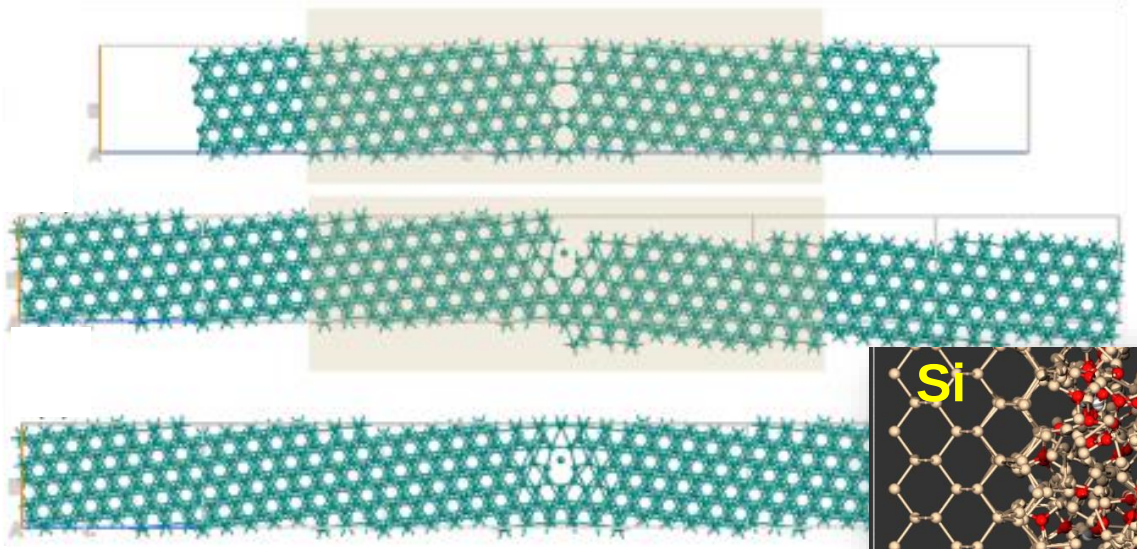
- Wire resistance increases sharply after 3nm node
- Cobalt doesn't help much
- Variability explodes at 2nm

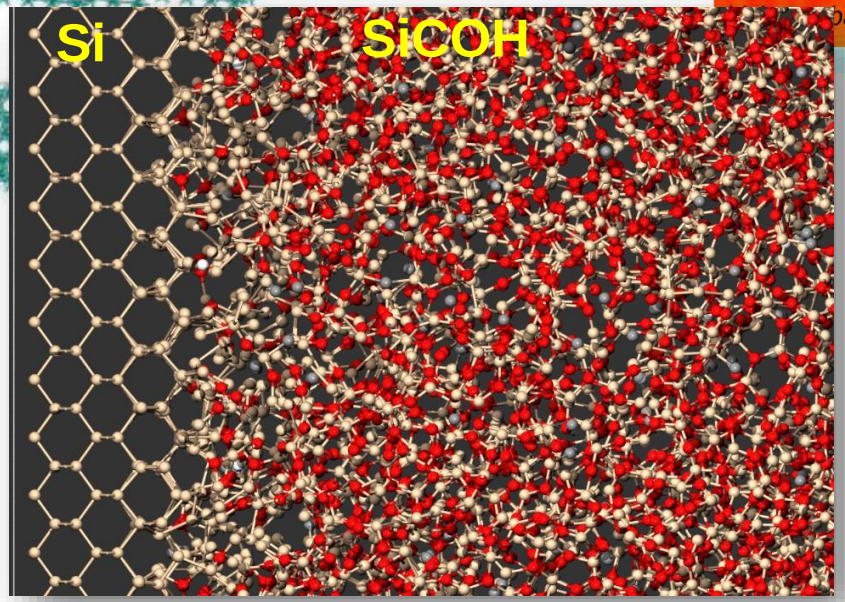
Outline

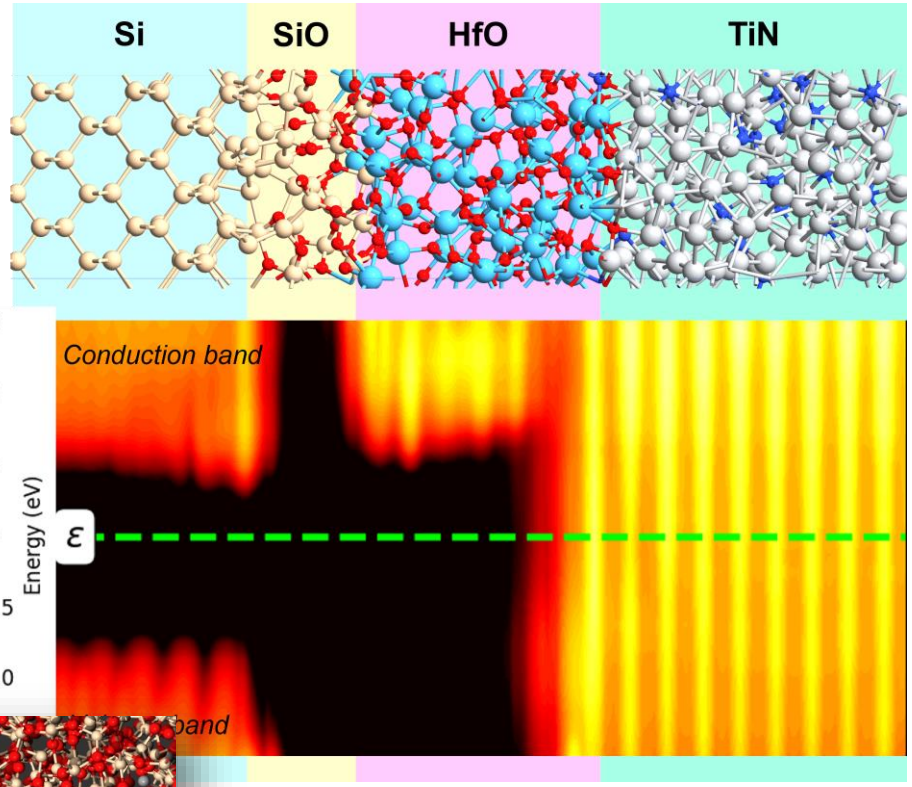
- Transistor evolution
- Interconnect evolution
- **Ab-Initio material engineering**
- Industry logic roadmap
- DTCO + STCO
- Summary

Ab-Initio Material Engineering

Electron scattering at grain boundaries in narrow wires







Porous dielectrics:

- Permittivity vs
- Mechanical strength

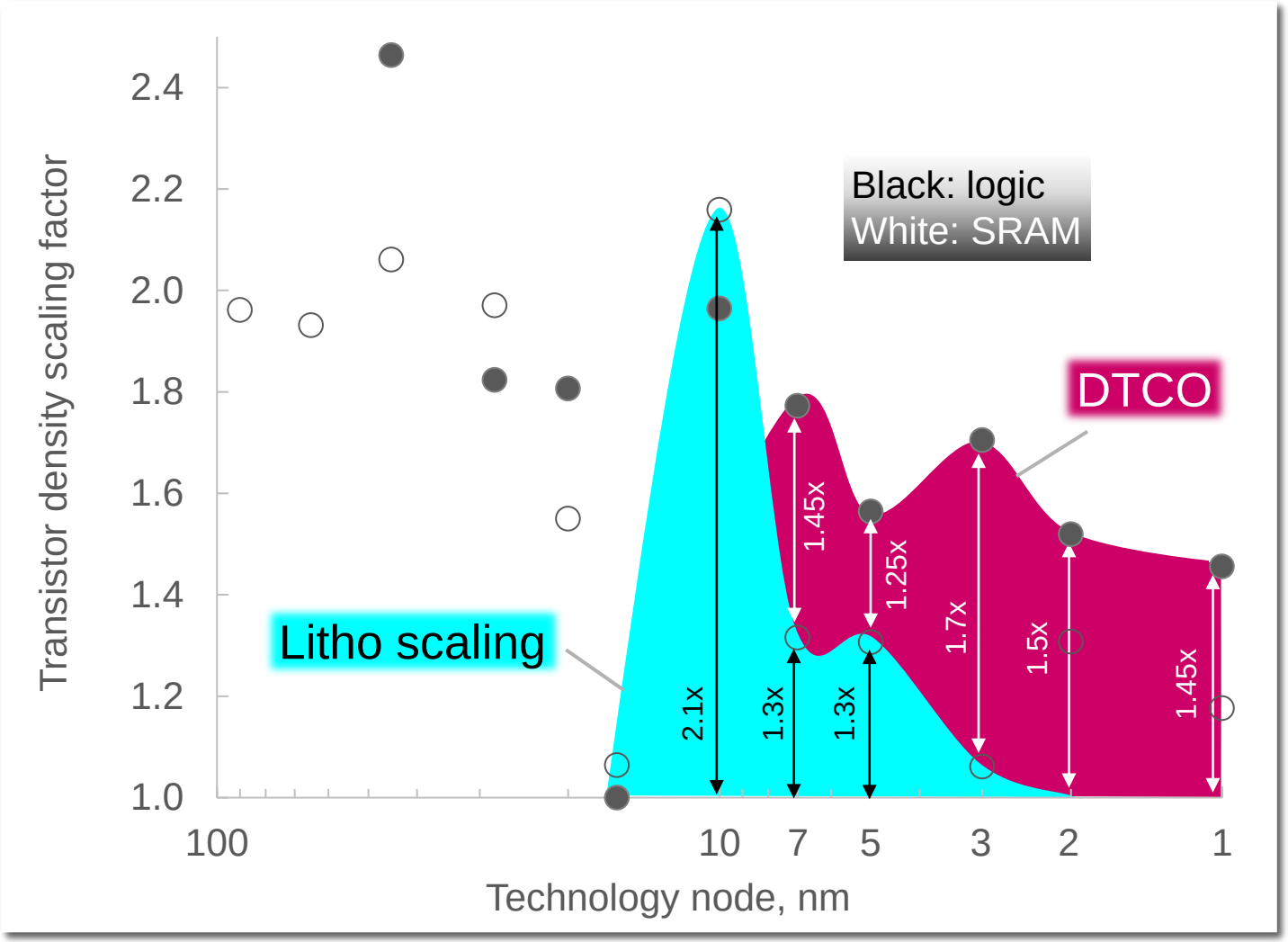
HKMG stack engineering:

- VT
- Leakage
- Remote Coulomb scattering

Outline

- Transistor evolution
- Interconnect evolution
- Ab-Initio material engineering
- **Industry logic roadmap**
- DTCO + STCO
- Summary

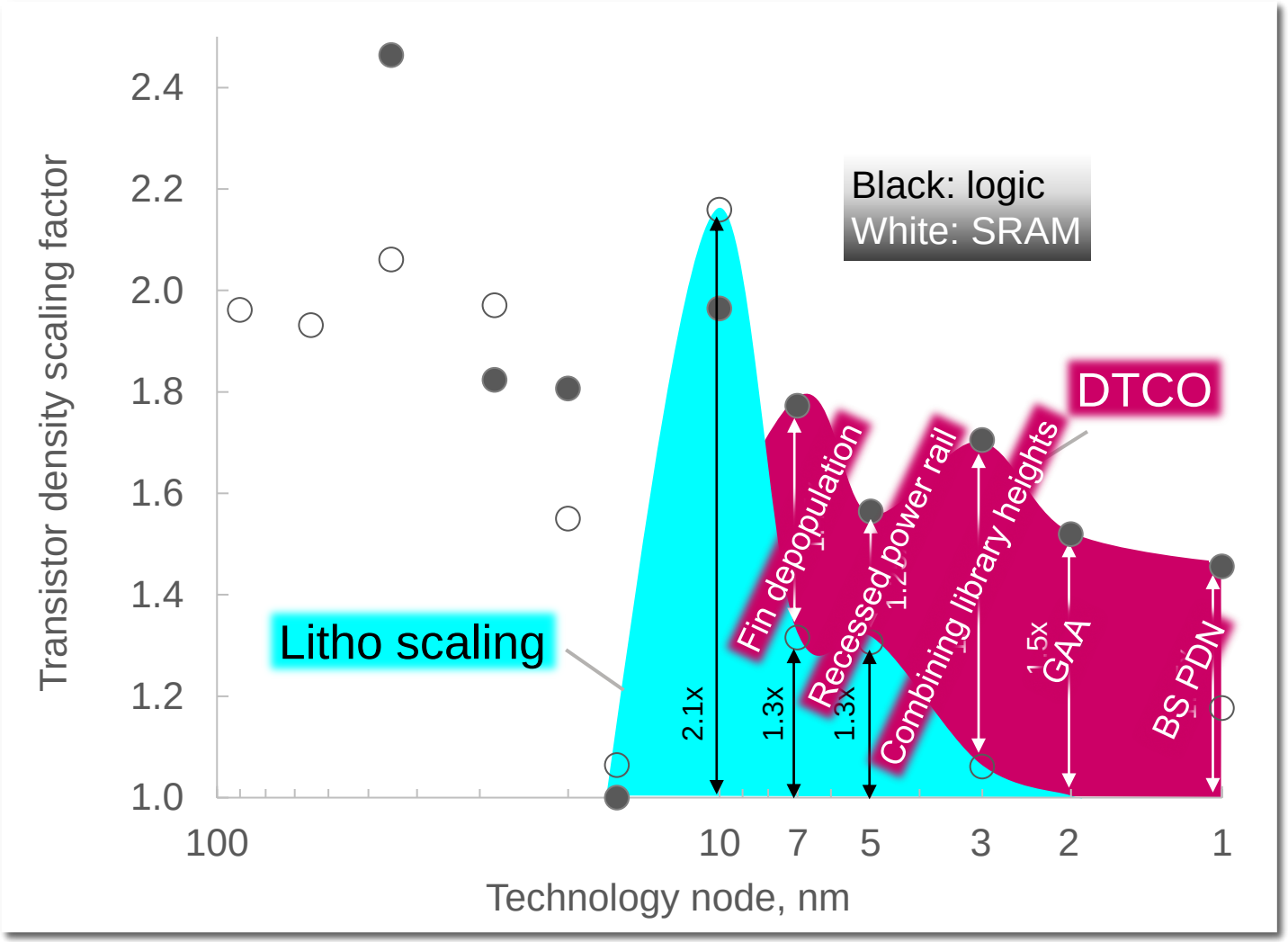
Historic and Projected Evolution of Transistor Density Scaling



Transistor density scaling between nodes for logic and SRAM: S.-Y. Wu (TSMC), IEDM 2019

- Transition from blue color to purple shows foundry transition from litho scaling to DTCO
- SRAM bitcell density is driven by lithography scaling down to 5nm node
- At 3nm node, SRAM bitcell has no scaling
- Starting at 2nm node, SRAM bitcell benefits from GAA
- Foundry is driven by DTCO beyond 3nm node

Historic and Projected Evolution of Transistor Density Scaling



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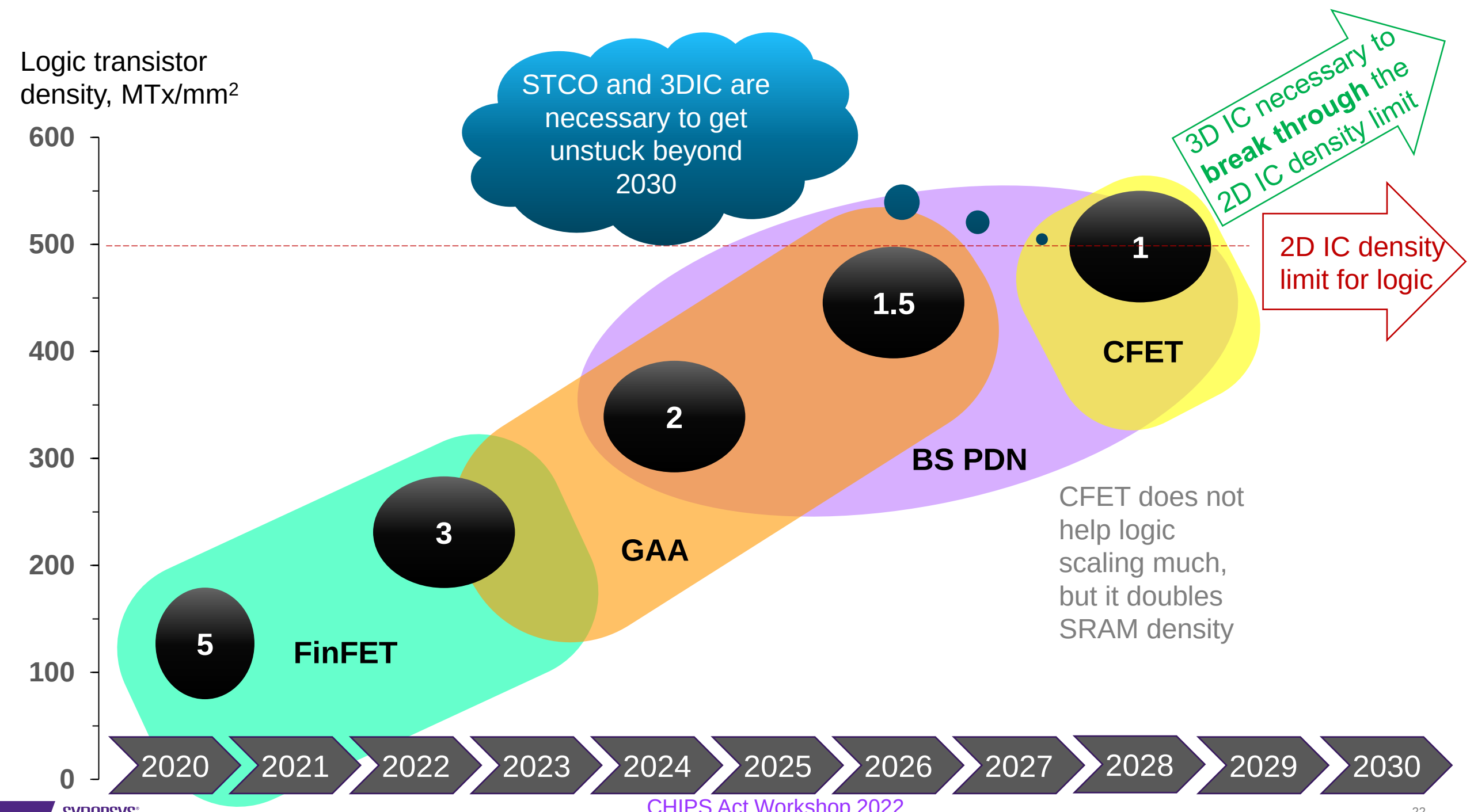
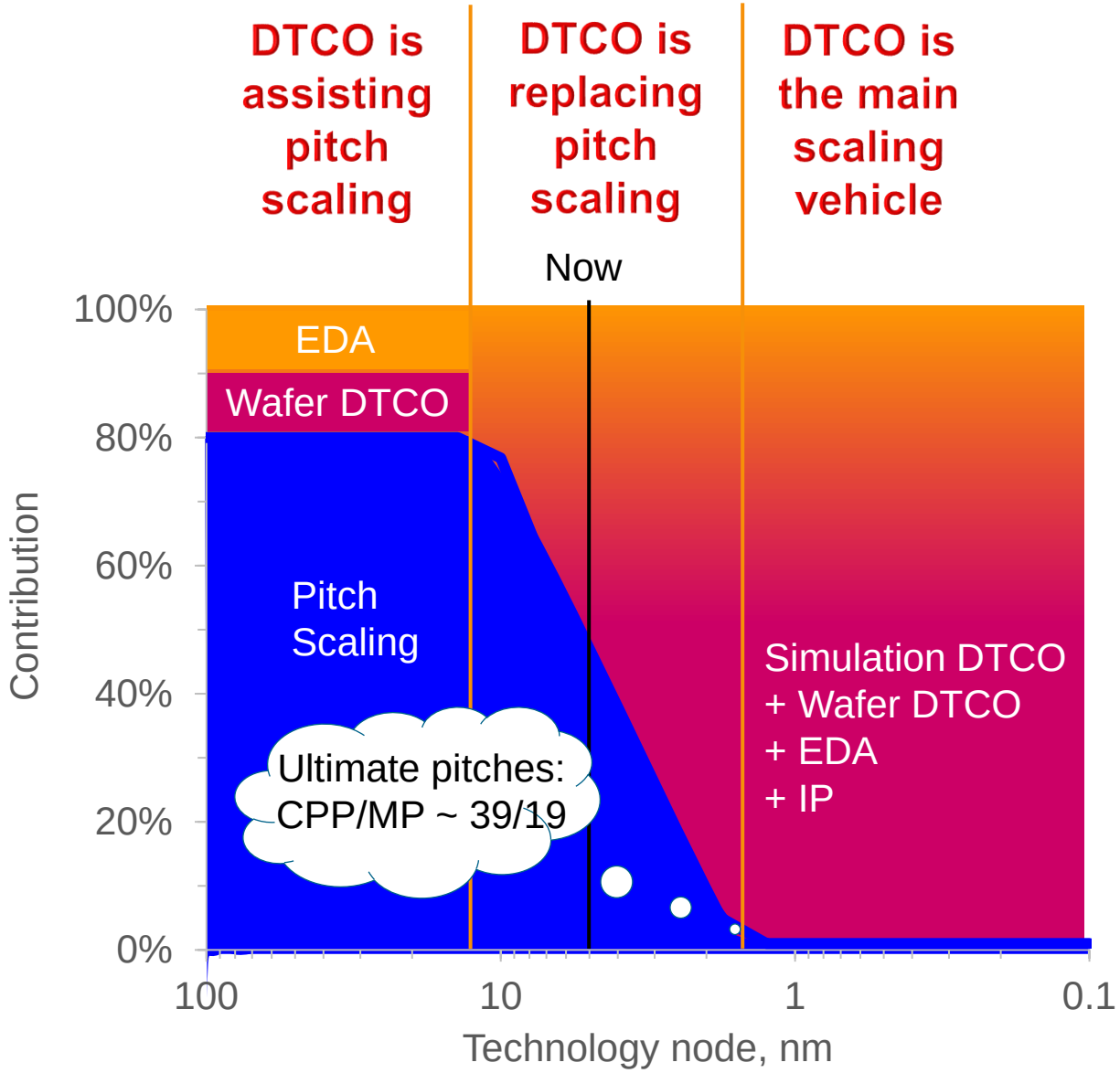

Logic transistor density, MTx/mm2
600
500
400
300
200
100
0
STCO and 3DIC are necessary to get unstuck beyond 2030
3D IC necessary to break through the 2D IC density limit
2D IC density limit for logic
1
1.5
2
3
5
CFET
BS PDN
GAA
FinFET
CFET does not help logic scaling much, but it doubles SRAM density
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030

Outline

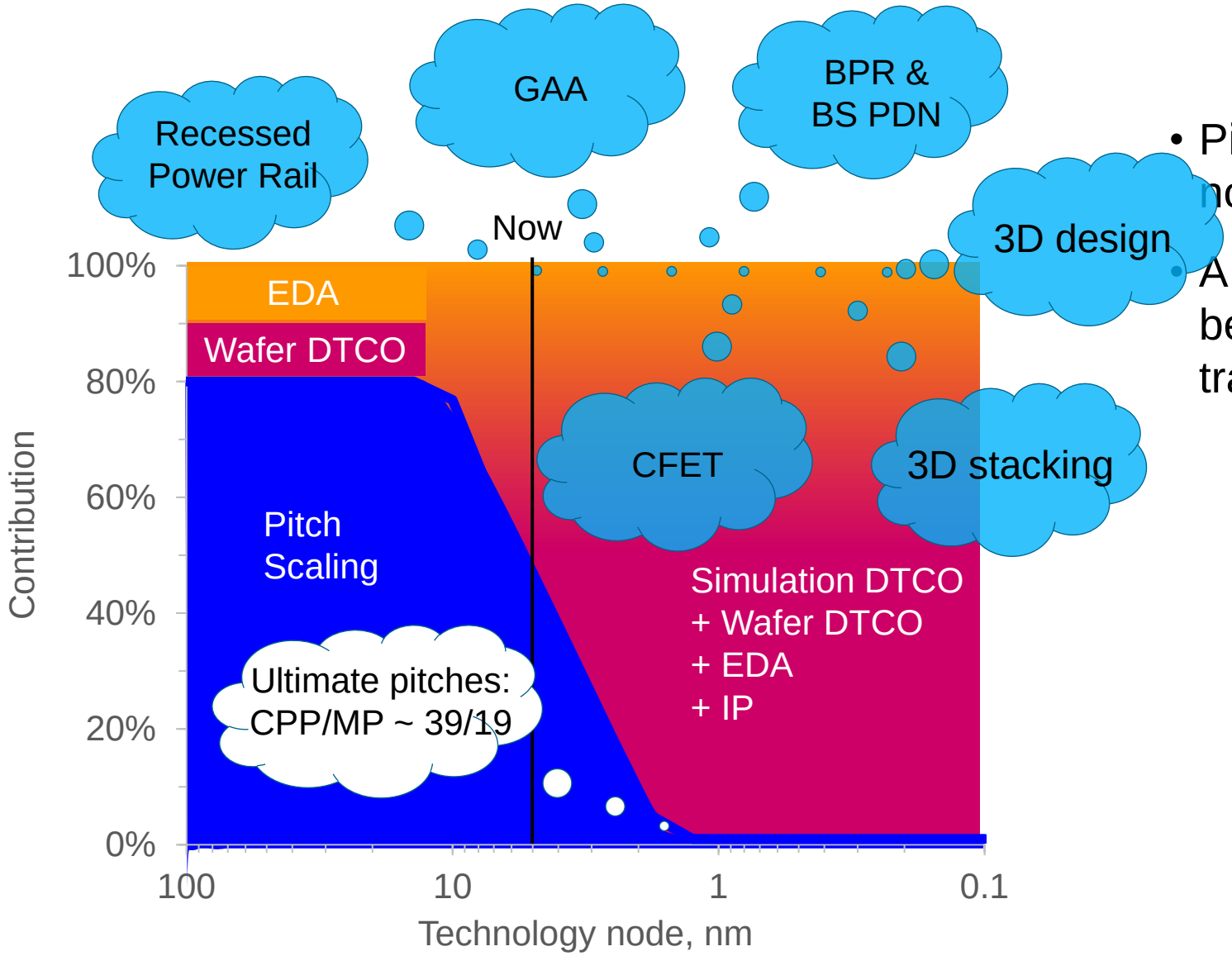
- Transistor evolution
- Interconnect evolution
- Ab-Initio material engineering
- Industry logic roadmap
- **DTCO + STCO**
- Summary

Evolution of the Key Vehicles of Transistor Density Scaling



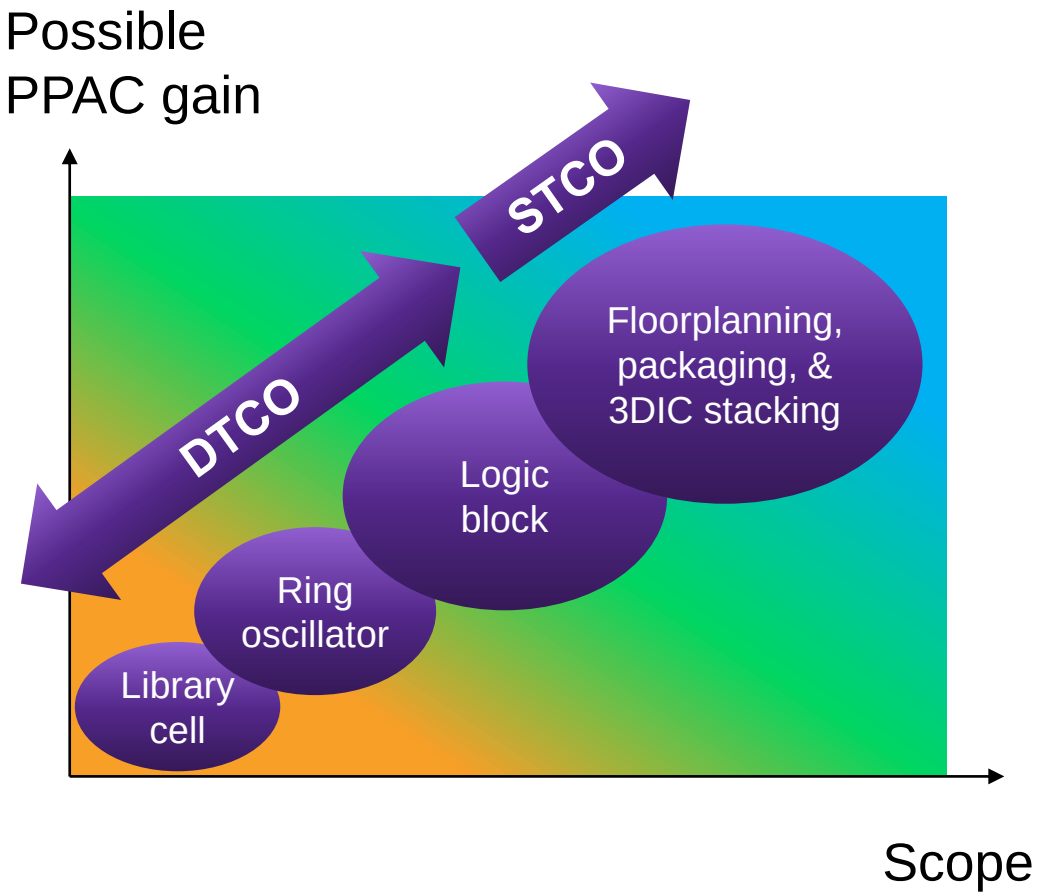
- Pitch scaling is expected to stop by 1nm node
- A combination of DTCO, IP, and EDA become the main vehicle of future transistor density scaling

Evolution of the Key Vehicles of Transistor Density Scaling



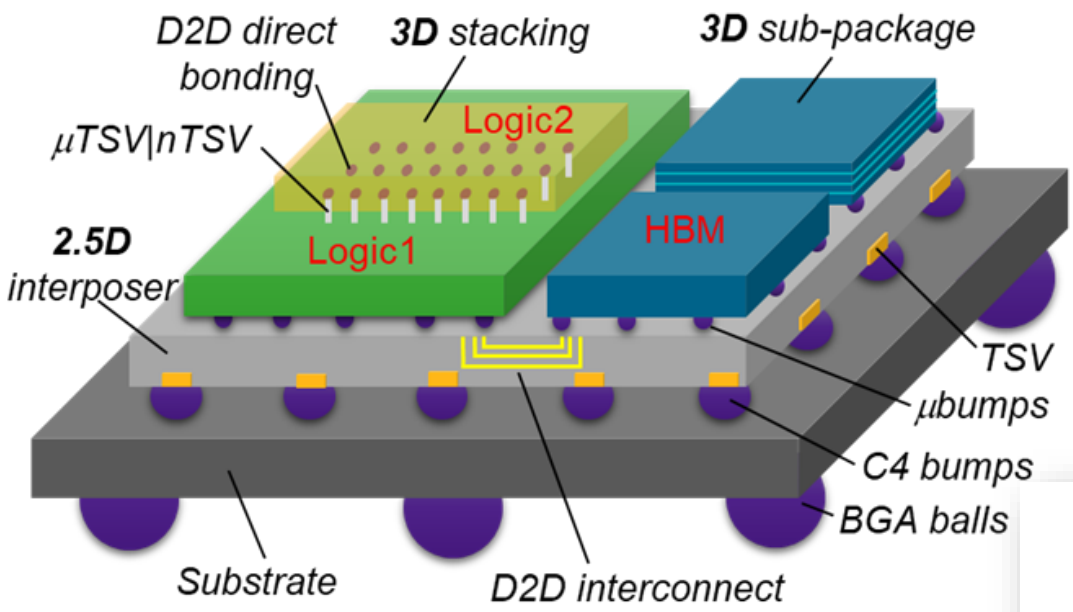
- Pitch scaling is expected to stop by 1nm node
- A combination of DTCO, IP, and EDA become the main vehicle of future transistor density scaling

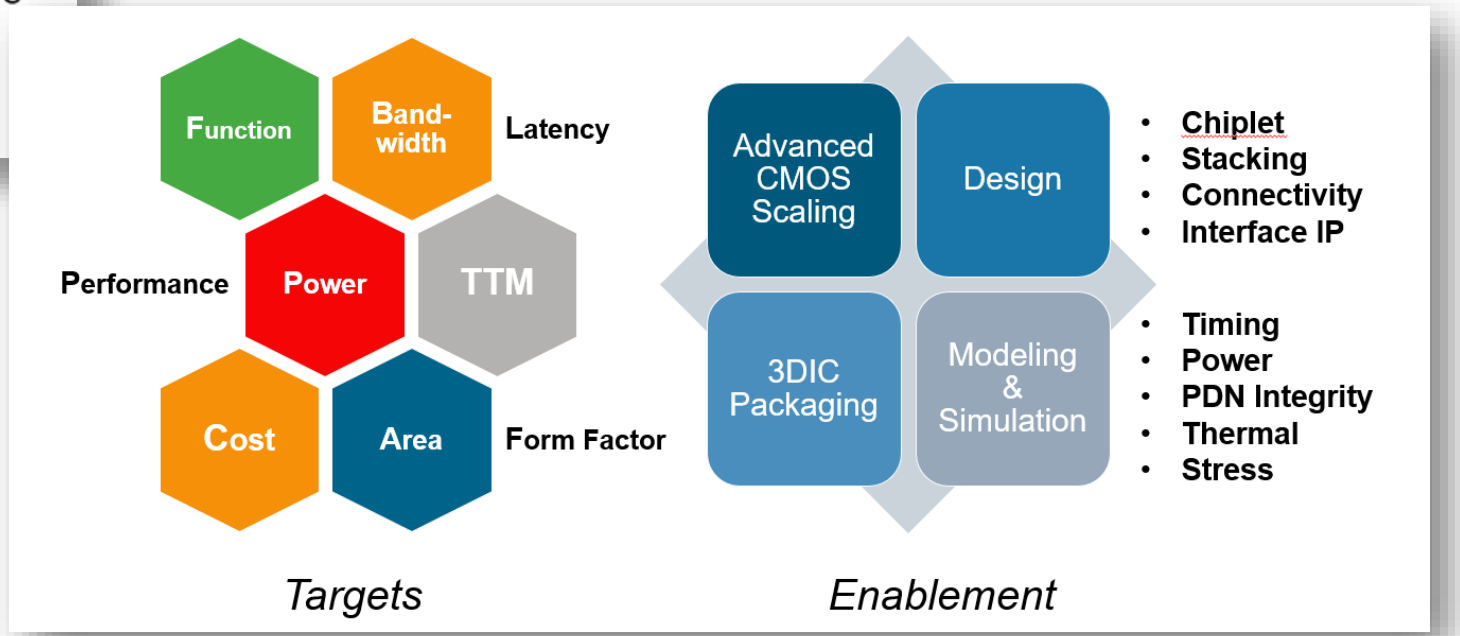
DTCO/STCO Scope



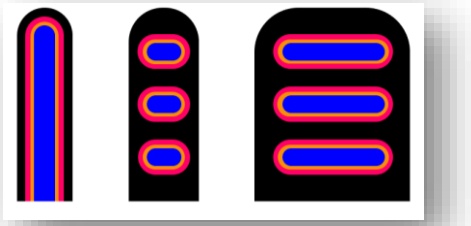
- PPAC (Power-Performance-Area-Cost) is the main technology metric
- Smaller scale PPAC analysis is faster and therefore enables evaluation of many technology and design options
- Larger scale DTCO/STCO analysis requires a larger effort, but enables bigger PPAC gains

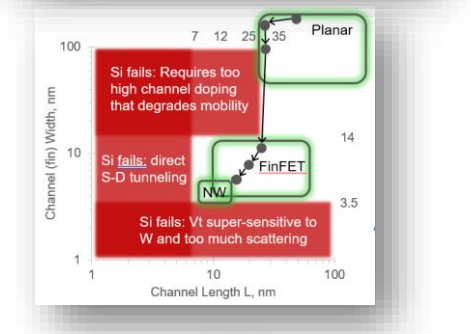
STCO for 3D IC Stacking

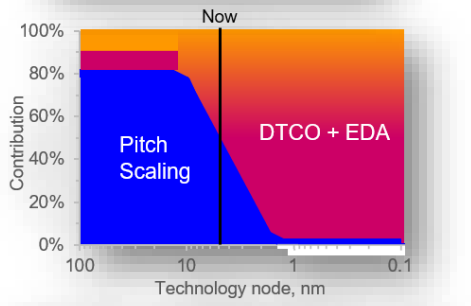


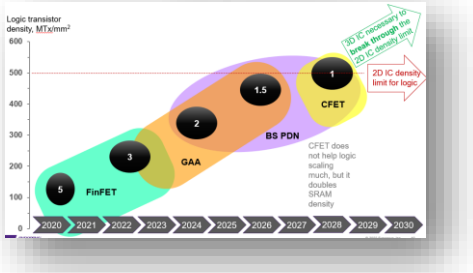


Summary









- Si is here to stay at least for the next 10 years, and likely more, so Silicon is the technology to invest into!
- Silicon CFET will take us to 500 million transistors per square millimeter for logic and 1 billion for SRAM, and that is the limit for 2D IC, limited by routing
- DTCO is already the main vehicle for transistor density scaling, and will keep Moore's law going through 2030, but it needs investment for better automation and turn-around time
  - Small Si transistors or larger high-μ transistors? – Only DTCO can tell the PPAC!
  - Tiny wires with high R or bigger wires with better R? – Only DTCO can tell PPAC!
- STCO, 3D IC stacking, and 3D place-and-route are necessary to go beyond 2D IC limits, and will provide a breakthrough beyond 2030. This requires a fundamental change in IC design paradigm, and requires investment!

Future of Simulation Driven Innovation in Nanotechnology Research

Prith Banerjee, Ph.D.
Chief Technology Officer, Ansys

September 8, 2022

Ansys

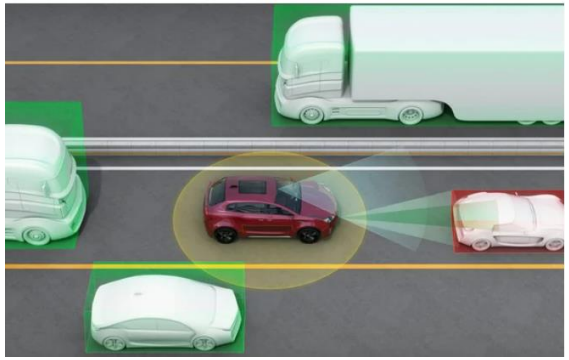
Brief Personal Background

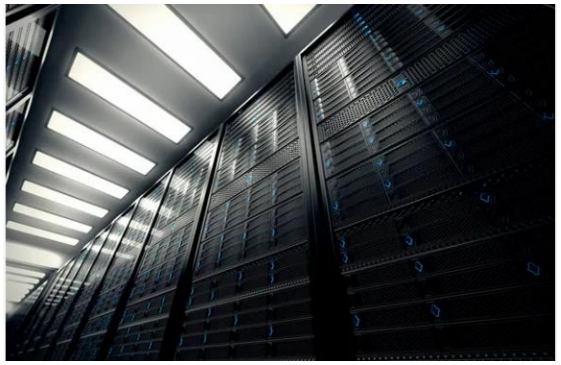
- 22 years in academia, 2 startups, 15 years in large companies
- Professor, Chairman, Dean at University of Illinois and Northwestern.
- Founder of Accelchip and Binachip
- Director of HP Labs, Managing Director of Accenture Tech Labs, CTO ABB, CTO Schneider Electric, and CTO Ansys
- Board member of Cray, CUBIC, and Turntide

- Fellow of IEEE, ACM, AAAS
- IEEE Taylor Booth Award, ASEE Terman Award
- 350 publications, 6 patents, 2 books
- Supervised 37 Ph.D. students, 40 M.S. students

Semiconductor Market Growth

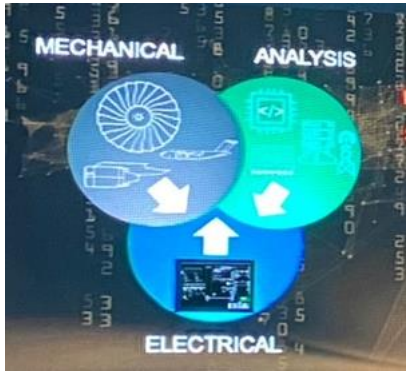
- Semiconductor market was $556 billion in 2021, is expected to be $600 billion in 2022 and will be **$1 Trillion by 2028** with an average CAGR growth of 10% (Global Semiconductor Industry Report 2022)
- The generational drivers for this are:
  - Autonomous Vehicles
  - 5G
  - Hyperscale Computing
  - AI/ML
  - IIOT





Increasing need to model interactions between Semiconductor, Mechanical, Electromagnetics, and Fluids

- Multi-physics simulation
- Electronic Systems Market growing to **$3 Trillion by 2028**



Multi-physics Simulation Portfolio at Ansys

INDUSTRIES	AEROSPACE & DEFENSE	AUTOMOTIVE	ENERGY	HEALTHCARE	HIGHTECH
SOLUTIONS	AUTONOMY	ELECTRIFICATION	5G	IIoT	
APPLICATIONS	CHIP PACKAGE SYSTEM	ELECTRONICS RELIABILITY	TURBOMACHINERY		
SIMULATION PLATFORM	**MATERIALS**	**CLOUD / HPC**	**OPTIMIZATION**	**PROCESS & DATA MANAGEMENT**	**MULTIPHYSICS**
SYSTEM OF SYSTEMS	**DIGITAL MISSION ENGINEERING**				
SOFTWARE & SYSTEMS SIMULATION	**DIGITAL TWIN**	**SYSTEMS**	**EMBEDDED SOFTWARE**	**SAFETY ANALYSIS**	
PHYSICS-BASED SIMULATION	**STRUCTURES**	**FLUIDS**	**ELECTRONICS**	**SEMICONDUCTOR**	**OPTICAL**	**3D DESIGN**	**PHOTONICS**

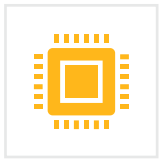
Ansys Long-Term Technology Strategy

NUMERICAL METHODS
- Accurate, fast, easy, robust
- Solver methods: direct, iterative
- Finite element, finite volume, IGA
- Implicit, explicit, hybrid, Bayesian

UI/UX AND VISUALIZATION
- Augmented Reality/Virtual Reality
- Ansys User Experience, Common UX, Common Components
- Reusable App Framework, MultiOS

MODEL BASED SYSTEM ENGINERING
- Collaborative System level modeling and 3D Sim
- Virtual Verification and Validation
- Lifecycle Trade Analysis & Optimization

MESHING / GEOMETRY
- Non- & Conformal Meshing
- Morphing, Immerse-Boundary
- Adaptive, Parallel Meshing



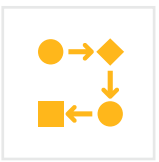
PLATFORMS/WORKFLOWS/DATA
- Multiphysics, Multi-domain, Multiscale
- Process Integration, & Optimization
- Data Management, Remoteable API

DIGITAL TWINS
- Data analytics/AI-ML
- Simulation-based, Hybrid
- DT for Design, Manufacturing, Operations

AI/MACHINE LEARNING
- Analysis Productivity
- Augmented Simulation
- Data Driven, Physics Informed, ML Based

CLOUD
- Private, Public, Hybrid
- Cloud First, App Streaming, Solver/UI
- Lightweight web browser for solvers
- Ansys Cloud Studio, Ansys Cloud Direct

ICME, ADDITIVE, SUSTAINABILITY
- ICME & Multiscale Modeling
- Additive Manufacturing, Additive Science
- Sustainability, Life-cycle-analysis



HIGH PERFORMANCE COMPUTING
- Task based, Shared memory, message passing
- Fine grain (GPU)
- Exascale and quantum computing

DEVELOPER ECOSYSTEM, SOLUTIONS
- pyANSYS Framework
- Solutions: EV, AV, 5G, NVH, Healthcare
- 3rd Party App Development

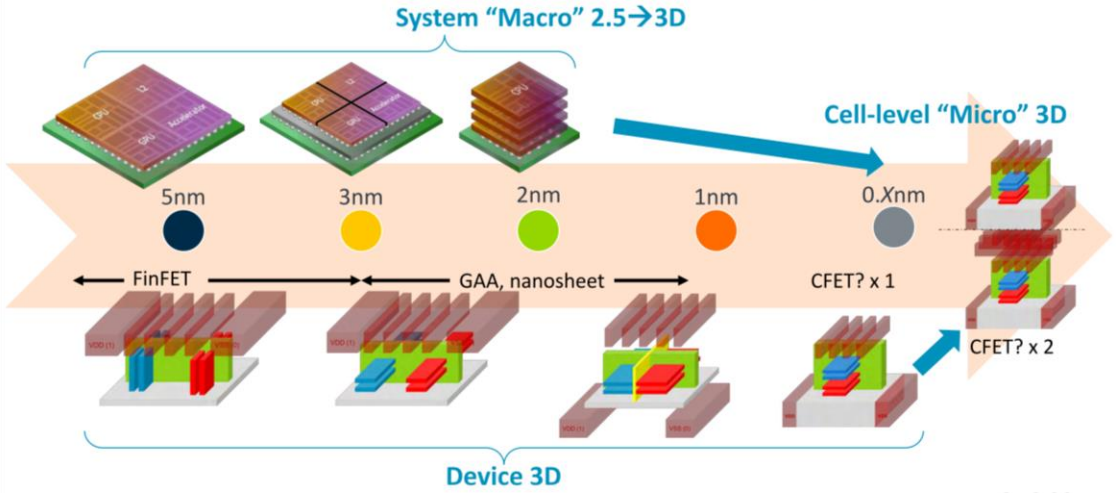
HEALTHCARE VERTICAL
- Biopharma, Medical devices & equipment
- Virtual Organ Modeling, In-Silico Trials
- Digital twins of devices, organs, avatars
- Clinical, Nonclinical apps

Future of Semiconductors and Electronic Systems

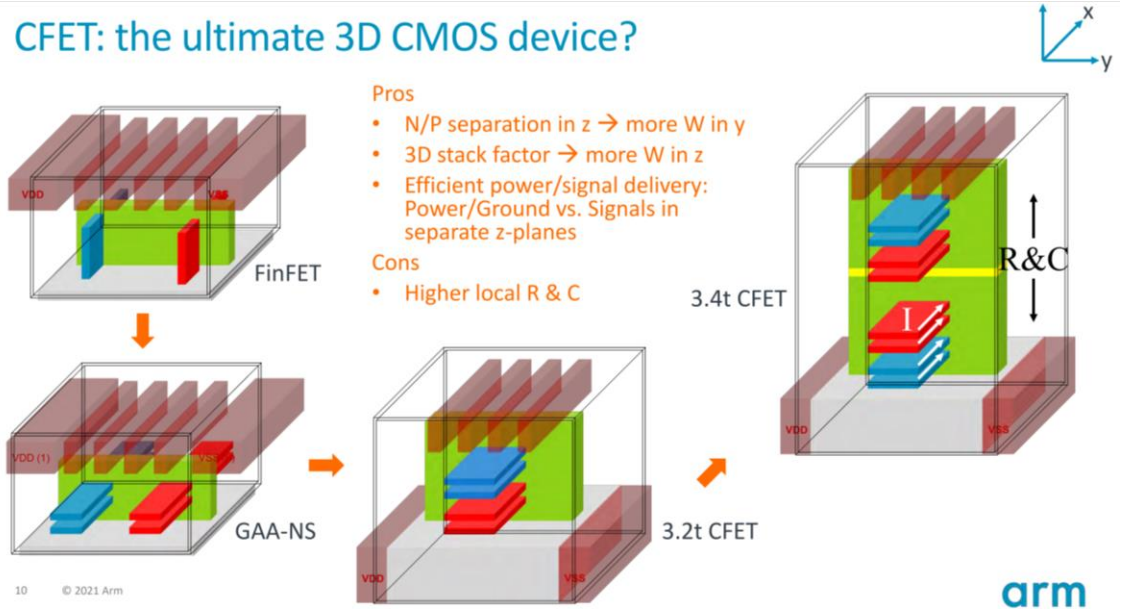
Ansys

Future of Semiconductors and Nanotechnology

"Moore's Law" – the next decade of scaling (and integration)



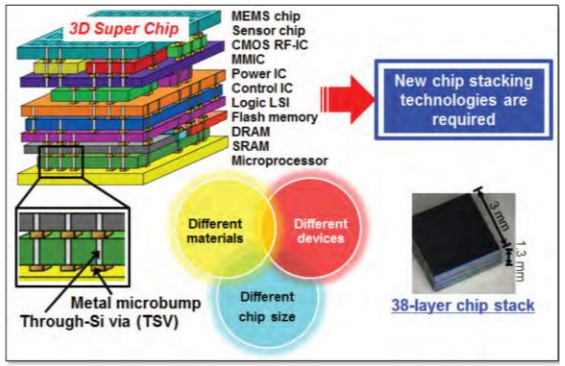
CFET: the ultimate 3D CMOS device?



Chiplets 1.0 (~10 years ago)

The future is up
- VNAND
- Image sensors

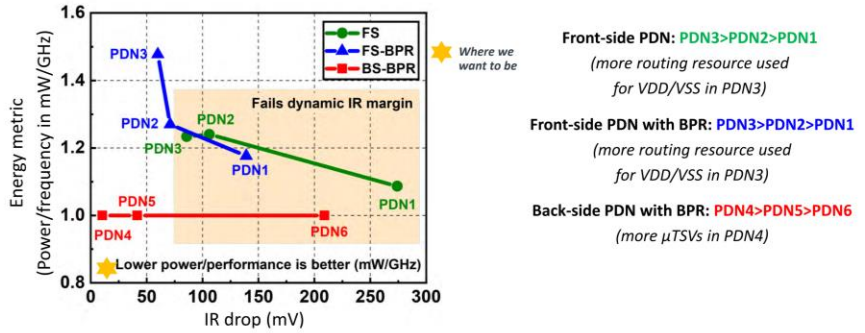
Challenges
- Manufacturing cost, complexity
- Design cost, complexity



Source: Heterogeneous 3D Integration - Technology Enabler toward Future Super-Chip, M. Koyanagi IEDM 2013

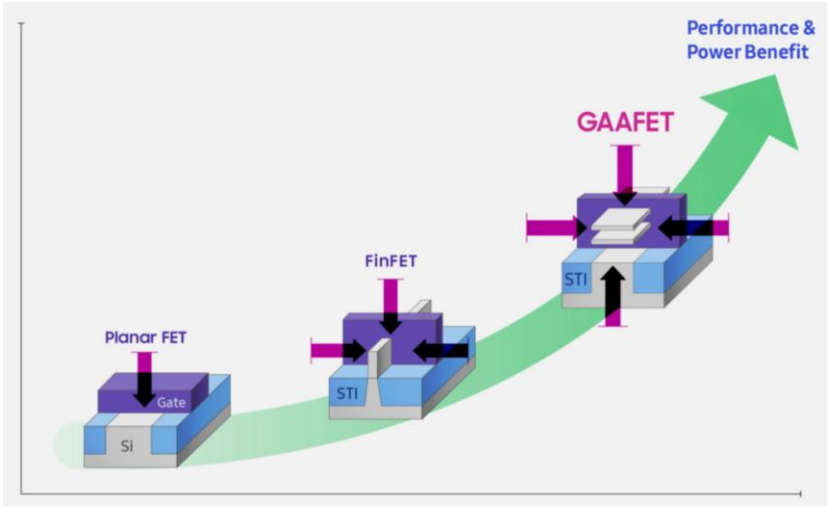
Summary slide: Front-side vs Back-side Power Delivery

- Back-side power delivery solves IR problems at narrow µTSV pitch <1µm



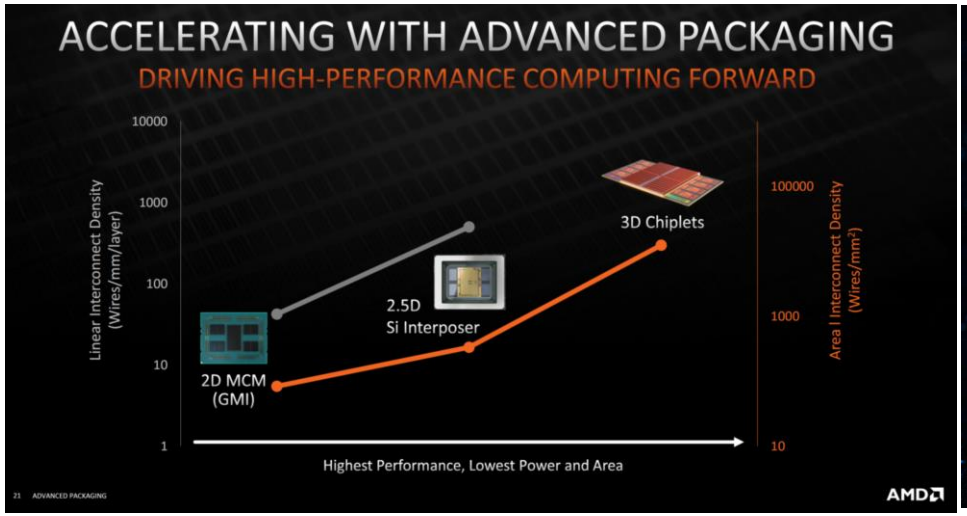
- Pay the price of performance and power to improve IR in front side power-delivery options
- Back-side power delivery decouples performance from IR drop management

New Semiconductor Technologies Drive Speed, Capacity, Reduce Power



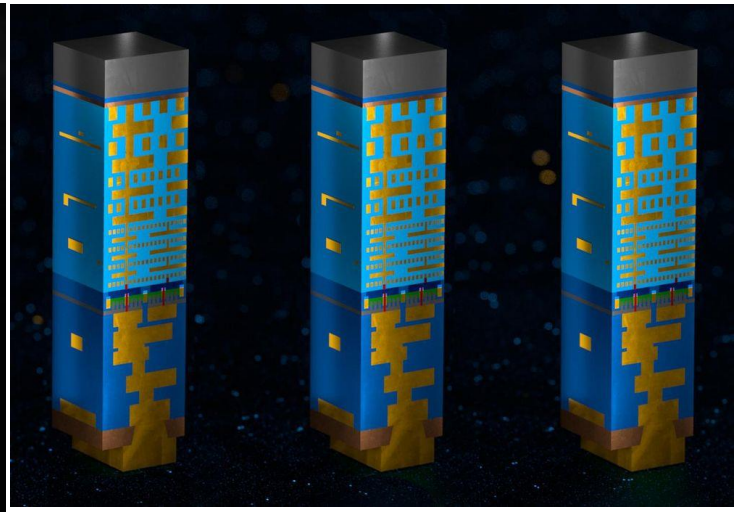
[Infographic] Reduced Size, Increased Performance: Samsung's GAA Transistor, MBCFET™ – Samsung Global Newsroom

TSMC, Samsung and Intel will deploy **new transistor technologies** at 3nm, starting in 2022/2023.



AMD Discloses Its Multi-Layer Chiplet Design Era, Starting With Zen 3 With 3D Stacked V-Cache Technology (wccftech.com)

2.5D and 3DIC enable continued scaling, higher performance and lower power usage

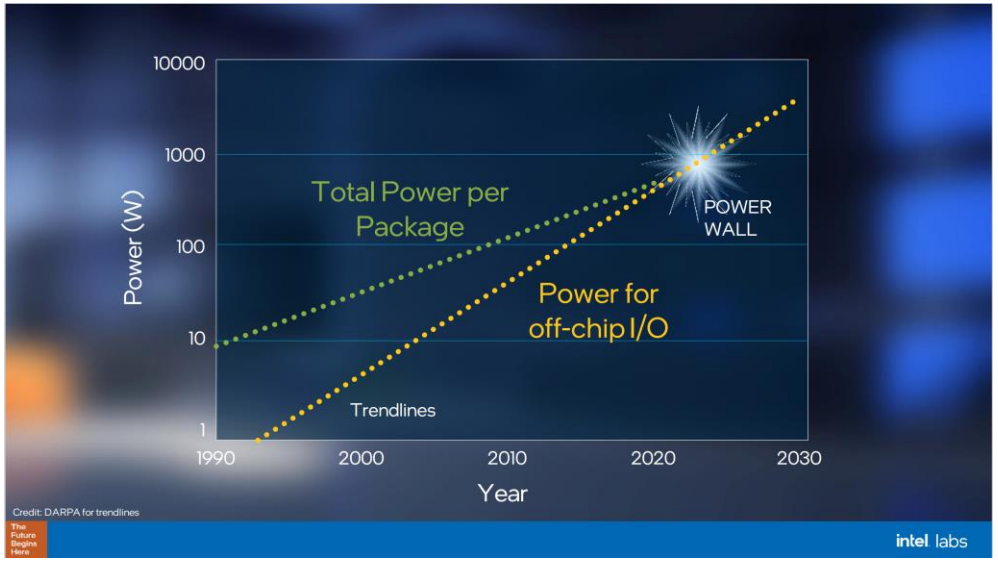


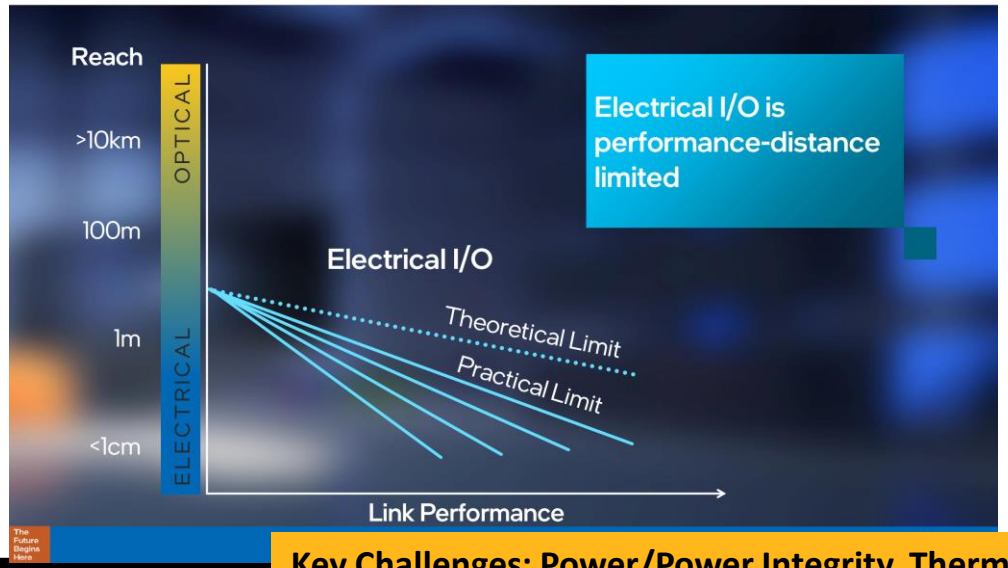
Intel: Back on Top by 2025? - IEEE Spectrum

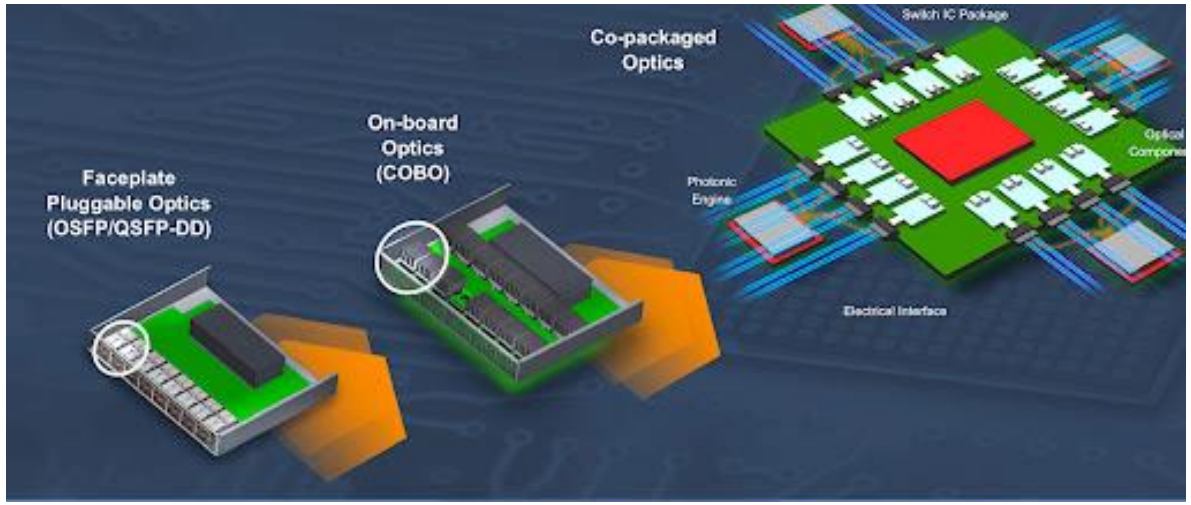
New **power delivery technologies** will enable higher compute densities. Intel's backside power delivery shown.

Key Challenges: Power/Power Integrity, Thermal/Mechanical, Electromagnetics/Signal Integrity
Complexity favors Ansys!

Compute Speed Is Driving Photonics to Augment Semiconductors







PowerPoint Presentation (ieee802.org)

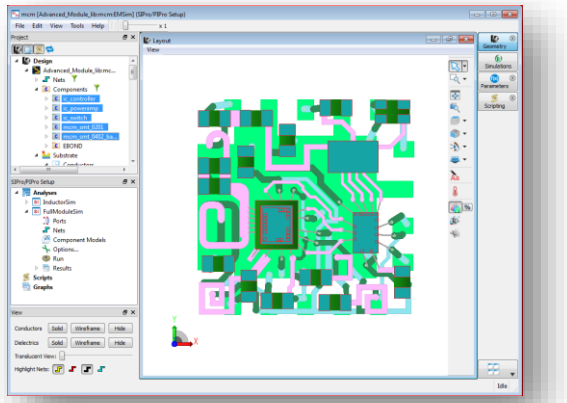
Co-packaged photonics and semiconductor chips in same package to reduce power and increase speed

CISCO, LUXTERA, ACACIA, intel, Hewlett Packard Enterprise, ciena, NOKIA, Inphi, NVIDIA, BROADCOM, JUNIPER NETWORKS

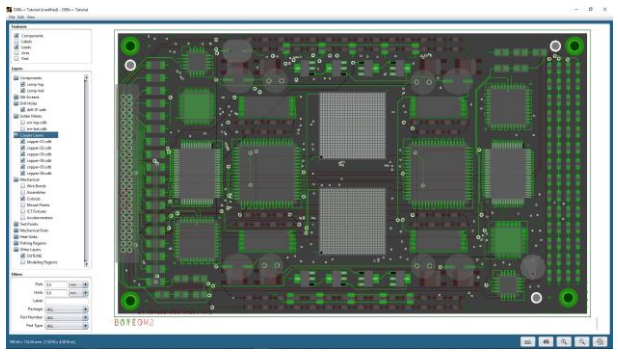
Key Challenges: Power/Power Integrity, Thermal/Mechanical, Signal Integrity/Electromagnetics/Photonics
Complexity favors Ansys!

https://newsroom.intel.com/wp-content/uploads/sites/11/2020/12/2020_LabsDay_Keynote-slides.pdf

Electronics, Semiconductors and Optics -- Unifying Themes



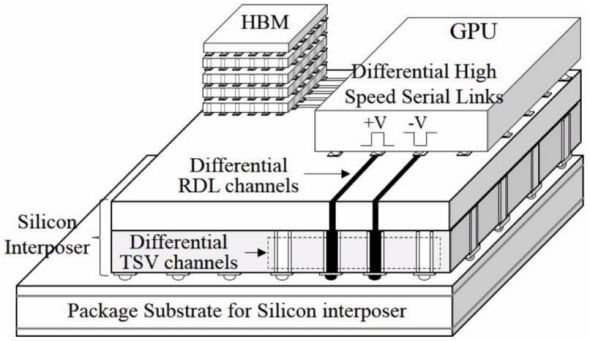
RF, PMIC, AMS



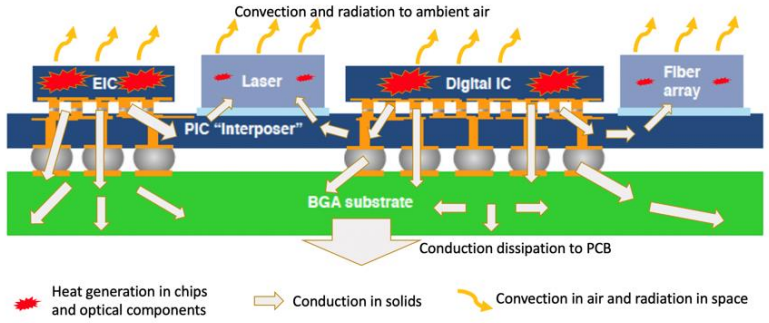
Chip-Package-Board

5G/6G and Edge IoT

HPC and Cloud



FinFET and 3D-IC



Co-packaged electro-optical

Automotive, Aerospace and Industrial

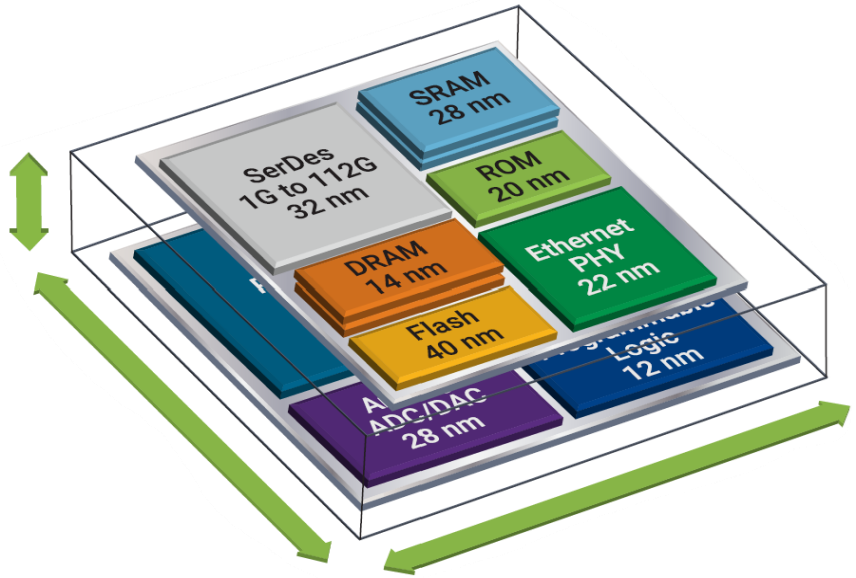
Multiphysics Solutions for SI/PI/TI/Reliability
(**Electromagnetics, Optics, Thermal**) x (Die, 3D-IC, Package, Board)

3D IC Simulation Solutions

Ansys

3D IC Engineering Challenges

Engineering Goal



Manage effectively **2.5D/3D Heterogeneous Integration** aiming at **maximizing Power-Performance-Area volumic density**

Engineering Requirements

- **Explore** design trade-offs in early stage with physics insights for optimal architecture selection
- **Implement** optimal design with sophisticated helpers (routers, design-rules checkers, …) and progressive design refinement capabilities
- **Analyze** thoroughly the performance against relevant operating conditions throughout the design process
- **Assess** chip-package to system-level electrical, thermal and structural integrities for reliable, safe and secure, semiconductors solutions
- **Ensure** optimal materials selection for reliability, cost and sustainability targets

3D IC | Chiplets Readiness

Soft IP Optimization

Engineering Goals

- Design for **worst-case workloads** and their increased peak-to-average power ratios, meeting timing closure challenges
- Remove **thermal-constrained performance restrictions** workarounds for better processing experience
- Drive physical implementation decisions for **power efficiency and yield maximization**

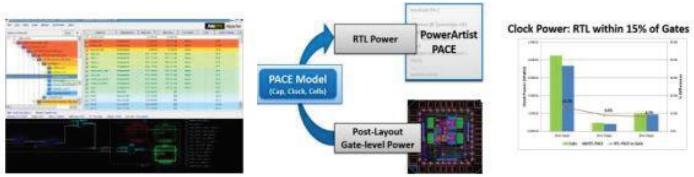
Ansys Solution

- **Accurate**, physically informed, **power profiling**
- Identification of **critical cycles and large current transients** to be optimized
- Connect to **emulators** for **higher power profiling coverage**
- Be able to **iterate early** on different options acting on clock gating

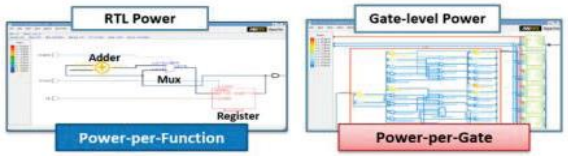
Benefits

- Idle **power reduction by 70%**
- Total average **power savings by 22%**
- **Turnaround time 20x** times faster than Gate-level Analysis

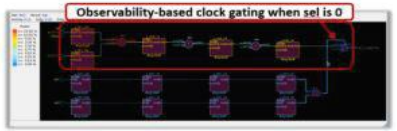
Register-Transfer Level (RTL) Power Budgeting



Comprehensive Power Analysis and Exploration

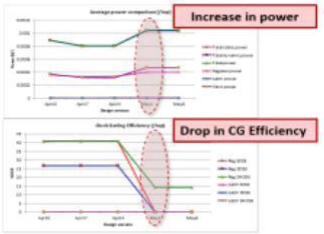


Analysis-Driven Automated Power Reduction



Early Power Profiling of System Activity

Regressions Based on Power Efficiency Metrics



RTL-Driven Power Grid

***Qualcomm Technologies** was able to **reduce dynamic power by 10 percent** through this approach. This is in a company (and a market) where reducing power is already an obsession.*

Chiplet Verification

Engineering Goals

- Improve top-level **power delivery network** and **signal nets** while verifying **dynamic voltage impact on timing**
- Optimize for **low power** and **power efficiency** with package-awareness, meeting **reliability** constraints
- Analyze **electrostatic discharge (ESD) protection** effectiveness, reduce **interference risks** and **side channel leakage**

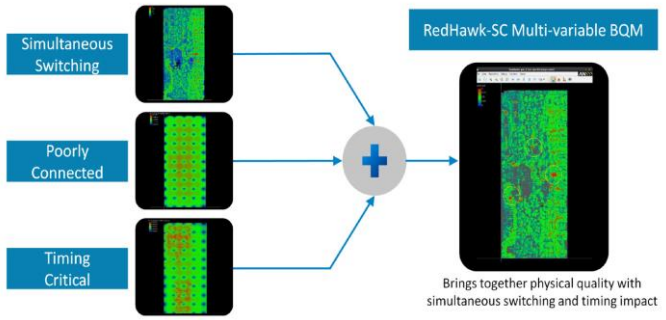
Ansys Solution

- **Supply network verification with chip-package co-analysis** and advanced **simultaneous switching noise** analysis
- Lower effective resistivity of **electrostatic discharge path** and analyze package-induced **electromagnetic coupling**
- Leverage capacity and performance of **elastic computing** and **big data analytics**

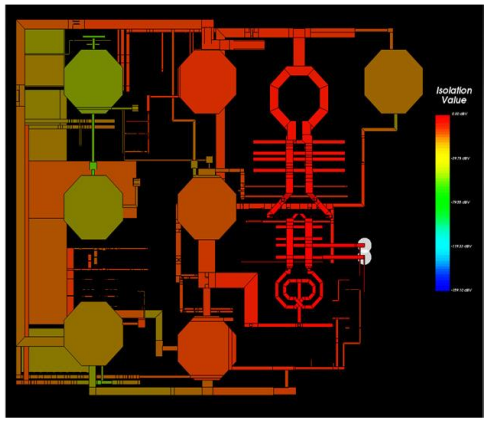
Benefits

- **Silicon first-time success**
- **Faster sign-off**, thanks to shorter engineering change order (ECO) loops and **faster ECO fixes with accuracy**

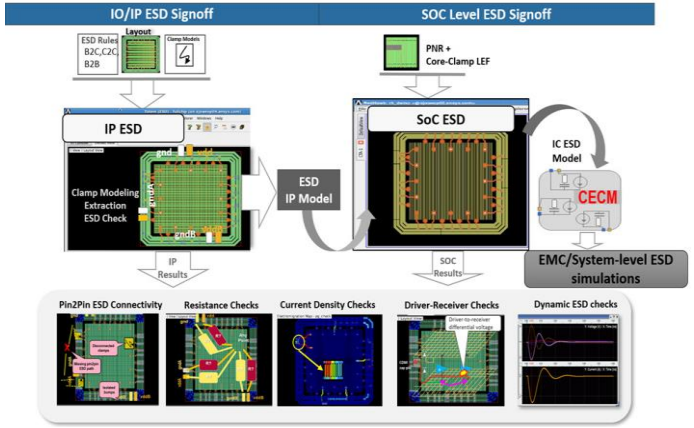
Multivariable Quality Metrics



Electromagnetic Crosstalk Analysis



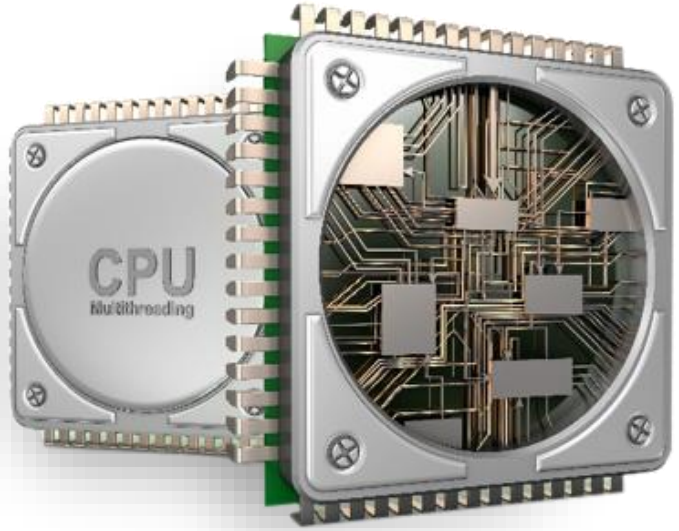
Chiplet level ESD Sign-off

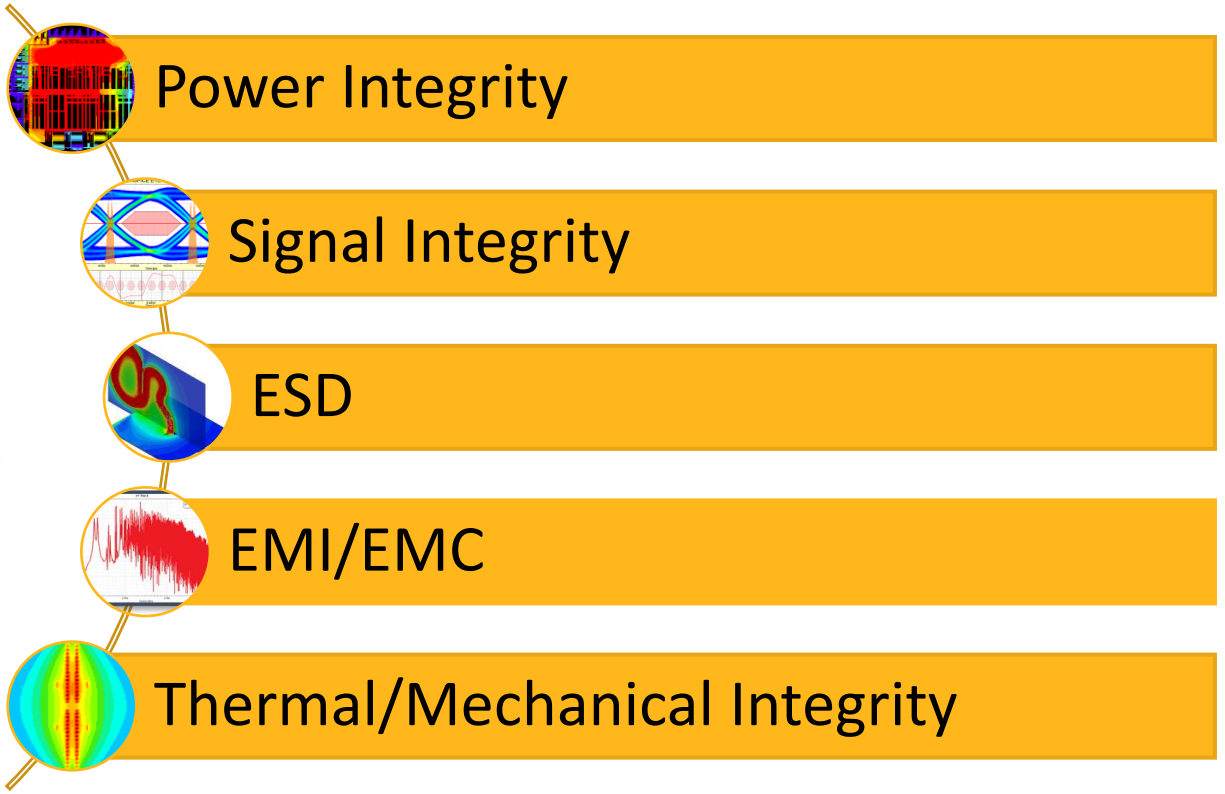


Chip-Package-System Design & Development

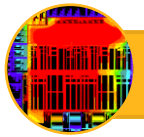
Simulation Capabilities Required To Realize These Benefits

Multiscale, multidomain and multiphysics simulation from the chip to the system





How Simulation Delivers The Required Capabilities



Power Integrity

Engineering Challenges

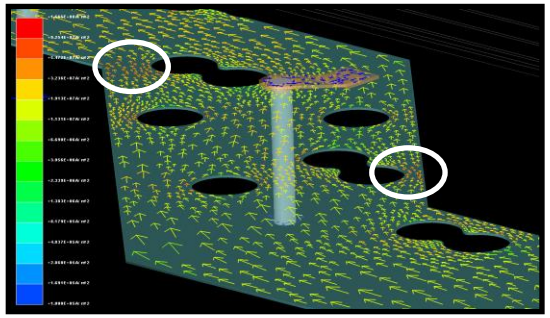
- Improve power efficiency
- Verify **P**ower **D**elivery **N**etwork
- Develop power planes and decoupling
- Meet emission compliance targets
- Minimize electromigration

Ansys Capabilities

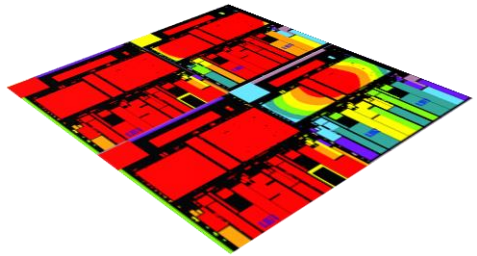
- Signoff PDN from transistor to system
- 2D/2.5D/3D IC support
- Chip aware system co-analysis
- System aware chip co-analysis
- Multiscale modeling : **C**hip **P**ower **M**odel, **C**ustom **M**acro **M**odel, **C**hip **M**odel **A**nalyzer

Example Outputs

- Transient power noise
- Current signature
- Voltage drop
- Impedance profile
- Optimized decoupling schemes
- Power/ground plane resonance
- Electrical models



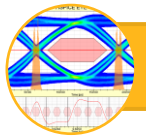
Current crowding



Voltage drop at IC level

Power supply noise vs time

How Simulation Delivers The Required Capabilities



Signal Integrity

Engineering Challenges

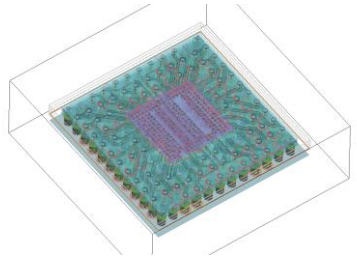
- Assess performance of multi-gigabit SERDES & DDRx memory
- Minimize crosstalk
- Meet standards requirements
- Achieve interface bandwidth

Ansys Capabilities

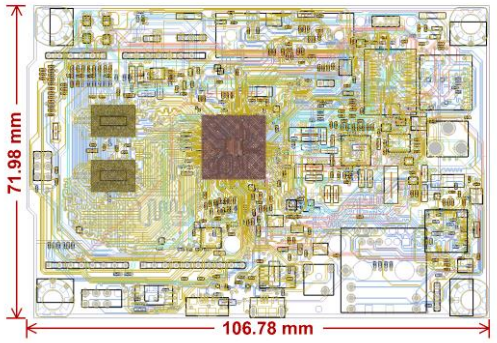
- 3D Full wave & hybrid EM solvers
- IBIS/IBIS AMI generation
- Power aware SI sign-off using **C**hip **S**ignal **M**odel
- Virtual compliance toolkits

Example Outputs

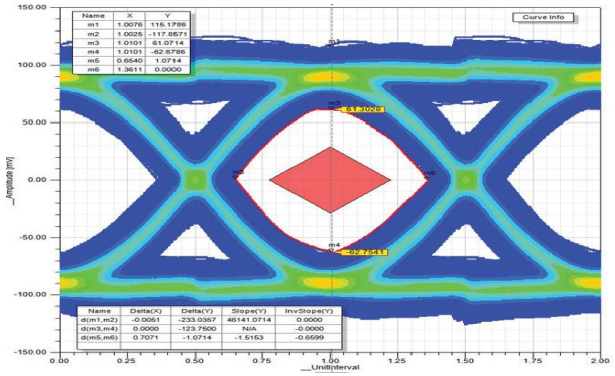
- S-parameters
- Eye diagrams, waveforms
- JEDEC, COM, USB sign-off report



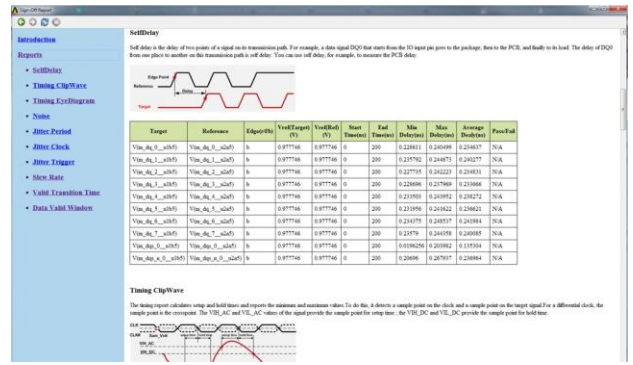
Multilayer BGA Package layout



Multilayer PCB layout

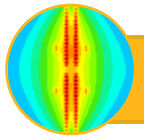


Eye diagram of a SERDES link



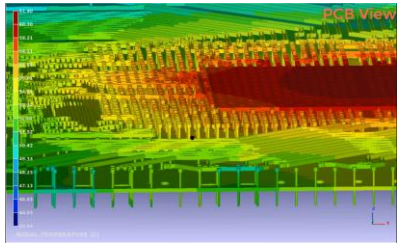
DRR Virtual Compliance sign-off report

How Simulation Delivers the Required Capabilities

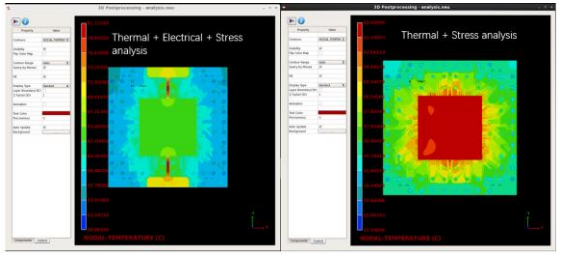


Thermal/Mechanical Integrity

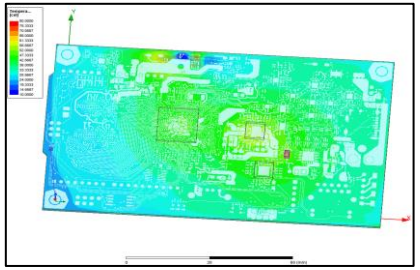
Engineering Challenges	Ansys Capabilities	Example Outputs
• FinFET thermal effects • Joule heating • Power dissipation • Thermal runaway • Thermal-induced stress	• Chip-level self-heat analysis • Chip-aware system thermal analysis • System-aware chip thermal analysis • CFD based thermal solver • **C**hip **T**hermal **M**odel • Prototyping with early power estimation	• Heat map • Temperature contours • Velocity vectors • Stress, deformation



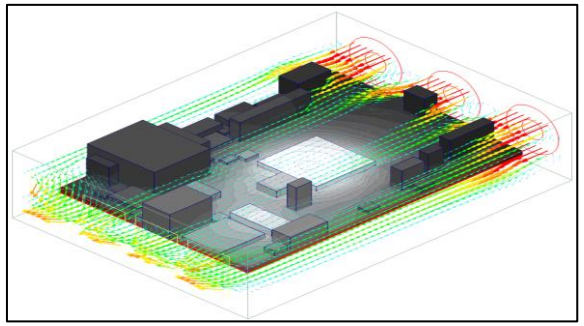
Full detailed thermal for chip package PCB



Electrothermal Joule heating with bump current



Joule heating with DC current



Full system level CFD thermal solver with air flow

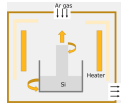
Semiconductors Manufacturing

Semiconductor Manufacturing Process Overview

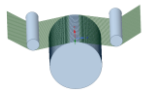
Blank Wafer Production

Printed Circuit Board Assembly & Testing

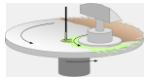
Silicon crystal growth



Ingot shaping and slicing

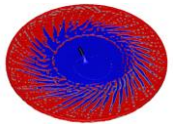


Wafer lapping, etching and polishing

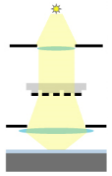


Oxidation

Coating application

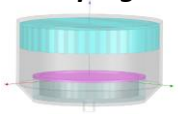


Photoresist exposure

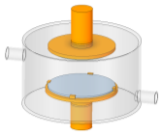


Etching

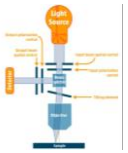
Doping



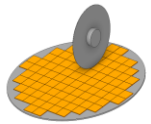
Layering



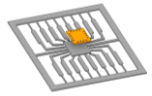
Inspection



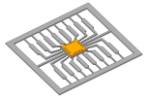
Wafer dicing



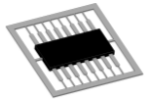
Lead frame mounting



Wirebonding, soldering

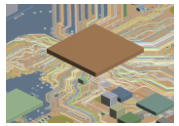


Molding

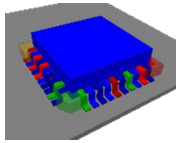


Trimming and forming

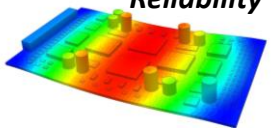
PCB Modeling



Mechanical Reliability



Shock and Vibration Reliability



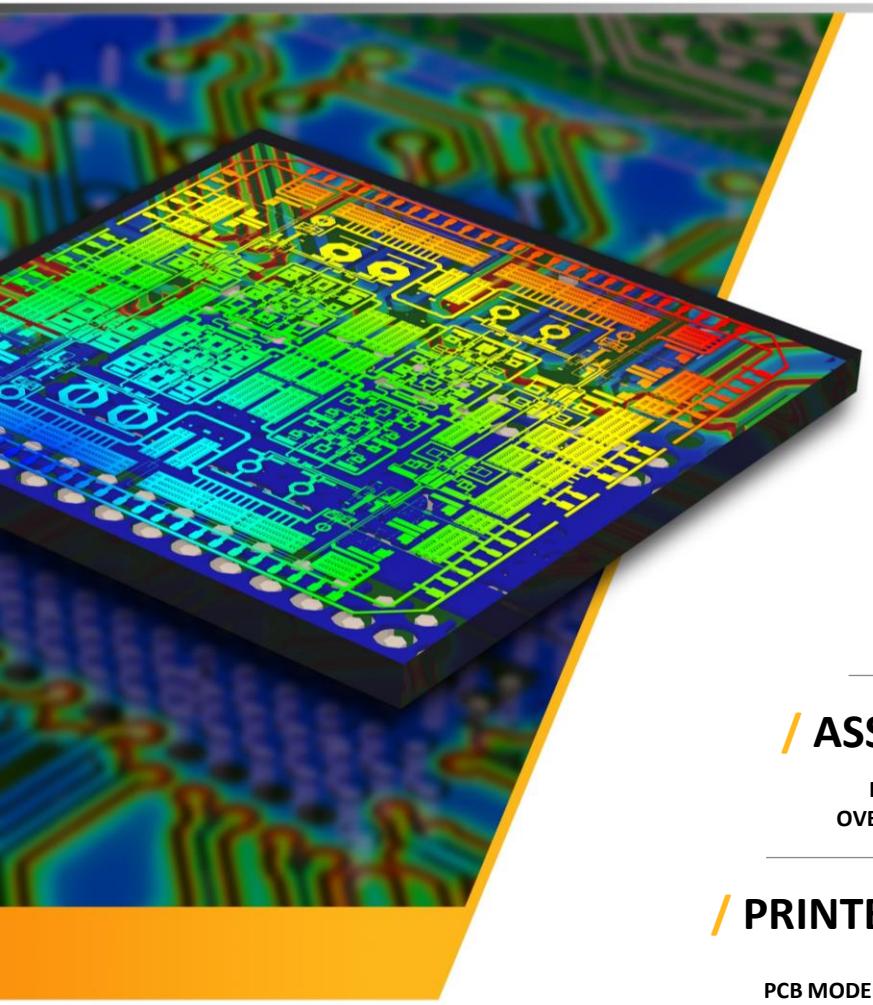
Raw Silicon Producers

Equipment Manufacturers and Chip Factories

Outsourced Assembly & Testing

PCB Manufacturers

How Simulation Delivers The Required Capabilities



BLANK WAFER PRODUCTION

POLYSILICON PRODUCTION	CRYSTAL GROWTH

SEMICONDUCTOR FABRICATION

CLEANING – WET TYPE (SPIN PROCESSOR)	CLEANING – SINGLE TANK TYPE	HEAT TREATMENT	COATING APPLICATION	WAFER DEFECT INSPECTION	ETCHING

REACTOR CONCEPTUAL DESIGN	REACTOR DETAILED DESIGN	ATOMIC LAYER DEPOSITION	EPITAXIAL GROWTH	FILM FORMING-VAPOR PHASE GROWTH THERMAL CVD	FILM FORMING-VAPOR PHASE GROWTH PLASMA CVD	FILM FORMING-LIQUID PHASE DEPOSITION

POLISHING	WAFER DEFECT INSPECTION	CLEAN ROOM HVAC DESIGN	AUXILIARY EQUIPMENT	WAFER HEATER	WAFER CHUCK	WAFER WARPAGE	DIE PREPARATION PROCESS

ASSEMBLY AND PACKAGING

REFLOW OVENS DESIGN	SOLDER REFLOW	BGA SOLDER REFLOW	ENCAPSULATION/EPOXY POTTING/UNDERFILL	LOW-K DIELECTRIC CRACKING	PACKAGE WARPAGE	THERMAL STRESS

PRINTED CIRCUIT BOARD ASSEMBLY & TESTING

PCB MODELING	PHYSICS OF FAILURE	SHOCK AND VIBRATION RELIABILITY	THERMAL CYCLING SOLDER JOINT FATIGUE	MECHANICAL RELIABILITY

Polysilicon production

Engineering Goals

- **Grow uniformly the rods** upon changing gas inlet position and mass flow rate of chemical reaction gases mixtures
- **Optimize reactor effectiveness** for production cycles

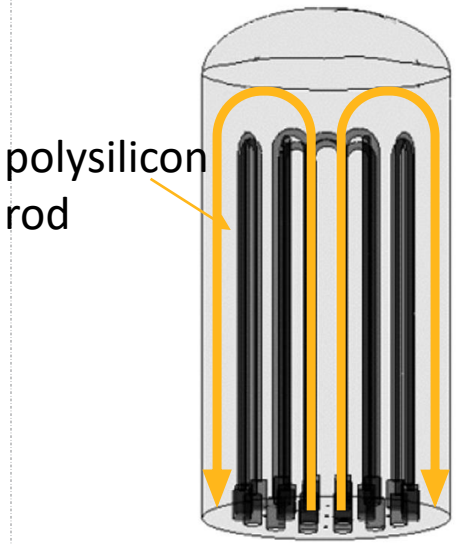
Ansys Solution

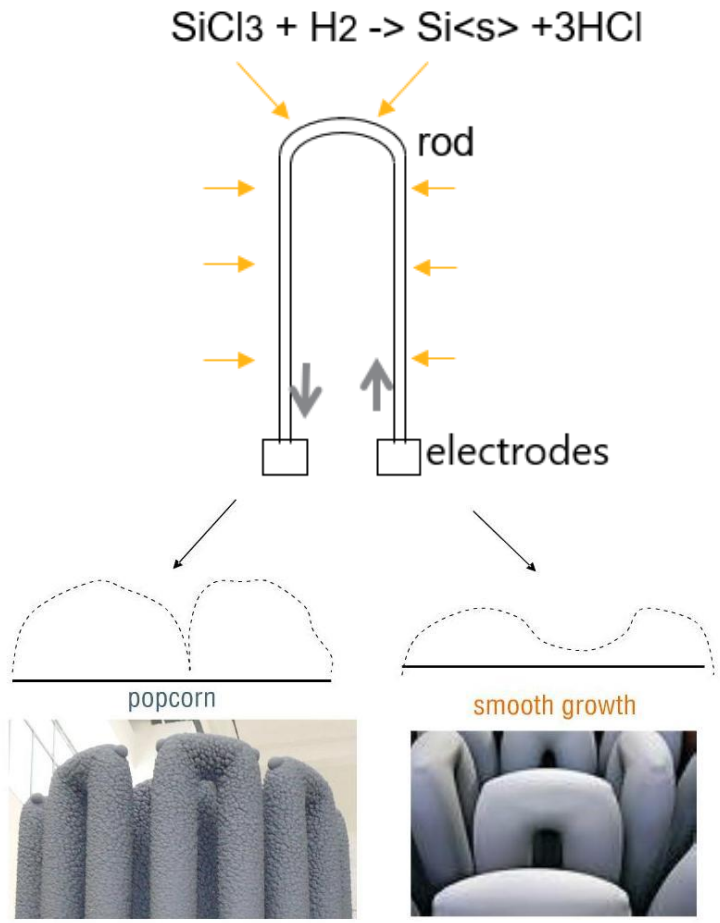
- A **Multiphysics-based approach** upon coupling **electromagnetics model** of the electrical heating distribution, modulated by current densities, to the **fluid dynamics model** of the rod growth, capturing convection, radiation and chemical reactions

Benefits

- **Reduced** prototypes number
- **Determination** of the cause of problems by understanding the flow in the furnace and the rod heating distribution

Haoyin, Ni, Shijie Lu, Caixia Chen, J Cryst. Growth 404





https://www.researchgate.net/publication/294579757_PhD_Thesis_UNDERSTANDING_AND_IMPROVING_THE_CHEMICAL_VAPOR_DEPOSITION_PROCESS_FOR_SOLAR_GRADE_SILICON_PRODUCTION

Crystal growth

Engineering Goals

- **Produce high purity and up to 12” large silicon ingots**
- **Suppress melt convection** effects, **guarantee crystal hypoxia with inert gases** and **prevent temperature oscillations** for a uniform dopant concentration and minimal impurities
- **Optimize crystal temperature distribution** (cooling rate, radial distribution) through radio frequency tuning and heater control

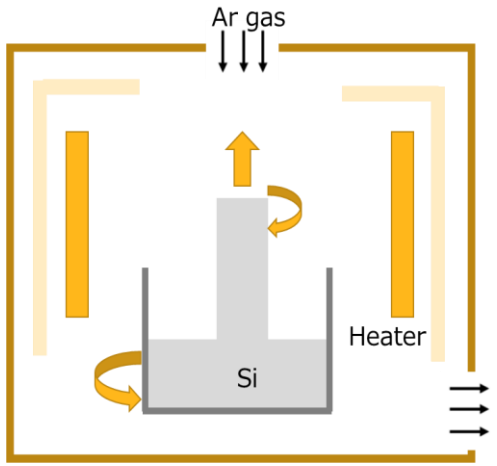
Ansys Solution

- **Tightly coupled electromagnetics-fluid dynamics** analysis for accurate modeling of the **melt flow and cooling rate for optimal melt transition shape**
- **High performance compute multiphysics** solvers assisted by **robust optimization algorithms**

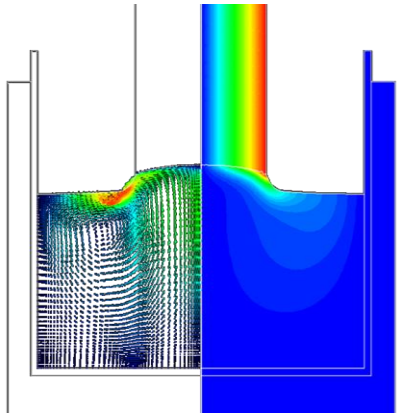
Benefits

- **Reduction** of experimental costs
- Ingot production **throughput increase**

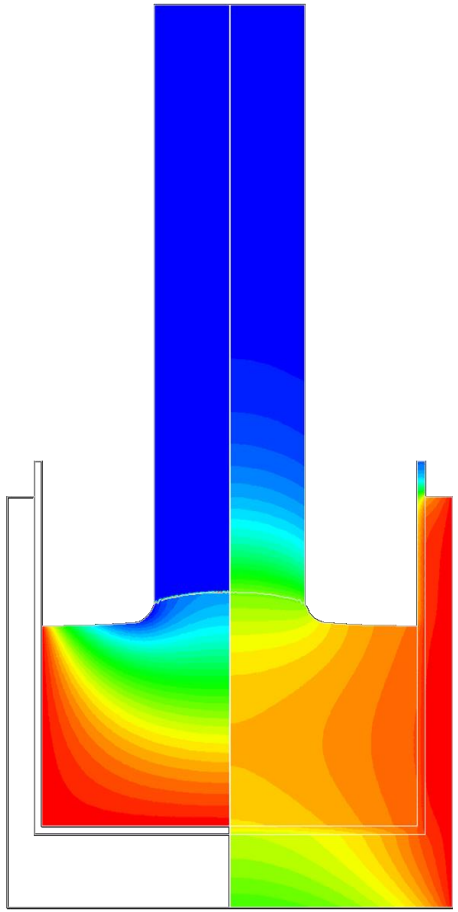
Czochralski (CZ) method



Melt convection velocity and pressure fields



Temperature distribution optimization



Big Bet Research Topics

Some Big Bet Research Ideas in Nanotechnology

- EDA Industry has solved the problem of design complexity by High-level synthesis, RTL Synthesis, Physical synthesis; works for digital systems, hard for analog systems
- Combined with Verification at each level (system, RTL, gate, physical)
- Can you develop completely automated synthesis from system level specifications (SysML 2.0) of complex electromechanical systems?
  - modeling multi-physics interactions between mechanical, fluids, electromagnetics and semiconductor technology
- Challenge of verification and validation is accurate, fast, robust and ease-to-use simulation
  - Multilevel (2nd order 3D PDEs, Reduced Order Models, System level simulation)
  - Multidomain (mechanical, fluids, electromagnetics, chemical, biological)
  - Multiscale (Integrated Computational Materials Engineering ICME, atoms -> systems)
- Hierarchical Verification and Validation Methods for complex systems
  - Multiphysics, multiscale, multidomain
  - How to best leverage AI/ML, HPC, and cloud in EDA synthesis and verification
  - Ease of use or workflows, accelerated synthesis and simulation, generative design
- How to develop accurate and fast digital twins of chips, subsystems, and systems? In design phase, manufacturing phase, operational phase
- How to apply Model Based Systems Engineering and concept of Digital Threads in the field of EDA?


Ansys

AMERICAN SEMICONDUCTOR ACADEMY

Introduction to the ASA Initiative*

Tsu-Jae King Liu

Dean and *Roy W. Carlson Professor of Engineering*
University of California, Berkeley

Chair, ASA Executive Committee

September 9 2022

NNCI Microelectronics/Semiconductor Research Community Virtual Workshop

*https://www.semi.org/en/workforce-development/ASA

A Growing Workforce Development (WFD) Gap

- The U.S. semiconductor industry employs roughly 300,000 workers with technical education and/or training.
  - Over 50% have a college degree and over 25% a graduate degree.
  - 20% only finished high school or do not have a high school diploma.
- U.S. universities/colleges presently do not graduate enough students to meet industry demand for new talent.
  (Additional sources of talent are needed, *i.e.*, via immigration and reskilling.)

- CHIPS Act programs will increase WFD need over the next 6 years, by >3400/yr ***additional*** new college engineering graduates, and >1200/yr ***additional*** new HS/CC technical graduates, on average.

→ Output of U.S. higher-ed. system for the industry should at least double!

Key Challenges for Meeting the WFD Need

1. **A largely invisible** (to students & public) **microelectronics industry**
2. **Aging infrastructure and faculty/instructor population**
3. **Lack of alignment between industry needs & higher education outcomes**
4. **Outdated microelectronics curricula**
5. **Pipeline inequality, limiting the size and strength of the talent pool**
6. **Talent retention (leaky pipeline)**

The American Semiconductor Academy (ASA) Initiative

Vision: Secure America's global leadership in semiconductor manufacturing, critical for long-term economic competitiveness and national security

Mission: Supply talent+innovation to fuel growth of U.S. semiconductor industry

- Broadly engage and empower engineering faculty to address WFD needs

Strategy: Foster collaboration between universities and partner with industry

- Attract students into semiconductor-related fields of study
- Develop knowledgeable & skilled graduates, from technicians to Ph.D.

Collectively Partnering with Industry for Greater Impact

American Semiconductor Academy

2400+ Member Companies

Academia: Rigorous education

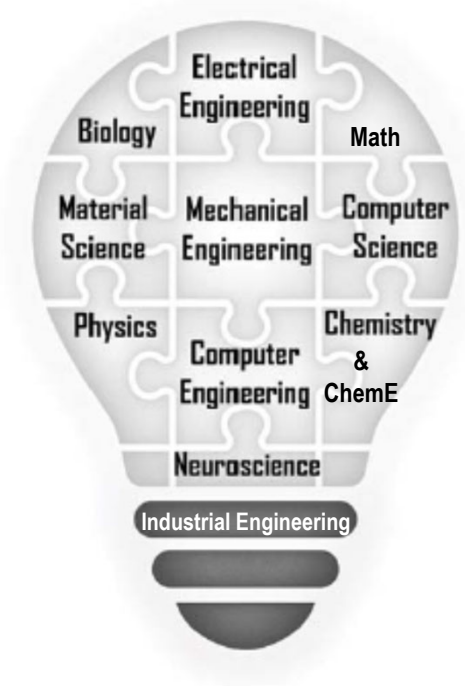
- ✓ Broad and diverse network
- ✓ Comprehensive STEM curricula
- ✓ Facilities for hands-on training
- ✓ Research programs – driving innovation

Outreach and Diversity, Equity & Inclusion (DEI) initiatives

Industry: Rewarding careers

- ✓ Deep industry connections
- ✓ Complementary workforce training
- ✓ Government connections
- ✓ Proven ability to effectively administer U.S. federal grants

Revitalizing the Microelectronics Curriculum



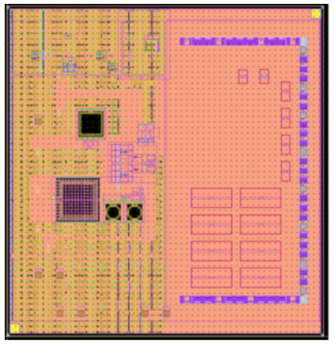
Knowledge	Skills
Packaging	Board-level integration
Heterogeneous Integration	Electronic Design Automation (EDA); Chip & System Test
Architecture	
Circuits	
Devices	Technology Computer Aided Design (TCAD); Fabrication and Characterization
Structures	
Materials	
Equipment	Maintenance & Repair
Computing, Data Analytics & Machine Learning	

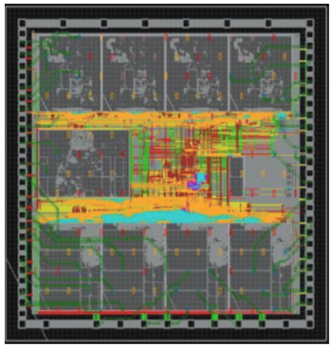
A modern curriculum should be **developed in partnership with industry** and shared across the ASA network to educate & train a broad diversity of students.

Democratizing Chip Design

- At UC Berkeley we have re-invigorated undergraduate and graduate courses to educate and train students in chip design and verification.
  - Students in a culminating ‘tapeout’ course collectively design a SoC in the course of one semester and send it out for fabrication at a foundry.

Final results of 2022 class project:
(2mm x 2mm chips)

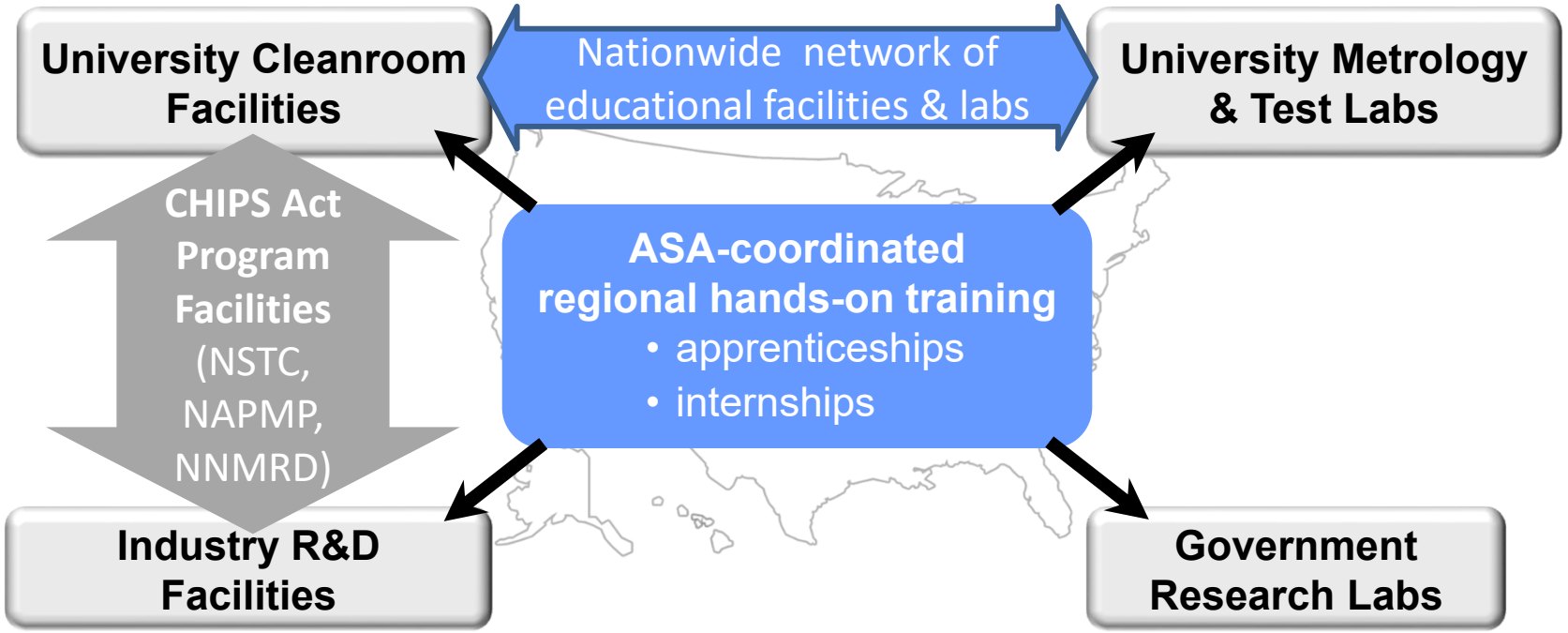




- **We are poised to scale up the impact of these curricular innovations through the ASA-SEMI partnership.**

Coordinating Hands-On Training in Regional Facilities

- To pique student interest in microelectronics, motivational course experiences and hands-on learning & training experiences are needed.

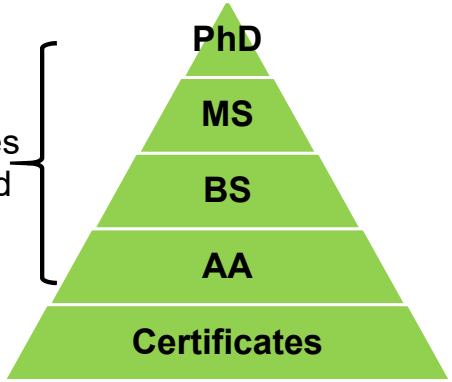


ASA Summary: Paving and Growing Diverse Talent Pathways

Knowledge	Skills
Packaging	Board-level integration
Heterogeneous Integration	Electronic Design Automation (EDA); Chip & System Test
Architecture	
Circuits	
Devices	Technology Computer Aided Design (TCAD); Fabrication and Characterization
Structures	
Materials	
Equipment	Maintenance & Repair

Computing & Data Analytics

degrees granted



Revitalized curriculum,

✓ accessible and open to students and working professionals nationwide

Coordinated Hands-on Training

- apprenticeships
- internships

New talent for U.S. semi. industry

Federal Funding via the CHIPS and Science Act of 2022

In addition to funding for CHIPS Act programs, the newly passed CHIPS and Science Act of 2022 appropriates **$200M over 5 years** for the NSF to promote growth of the semiconductor workforce.

Authorized activities include:

- new curricula and materials
- professional development programs
- design of, or direct support for learning experiences
- faculty hiring and academic research capacity building
- workforce pathway programs and partnerships
- graduate traineeships
- **creation of a National Network for Microelectronics Education**

Overview: National Nanotechnology Coordinated Infrastructure (NNCI)

Oliver Brand, David Gottfried, Azad Naeemi
Jamey Wetmore (ASU), Matt Hull (Virginia Tech)
NNCI Coordinating Office @ Georgia Tech

National Nanotechnology Coordinated Infrastructure

NSF

40+ Years NSF-Funded Nano Infrastructure

1977-1987
NRRFSS
National Research & Resource Facility For Submicron Structures
1 Site

1987-1994
NNF
National Nano-Fabrication Facility
1 Site

1994-2004
NNUN
National Nanotechnology Users Network
5 Sites

2004-2015
NNIN
National Nanotechnology Infrastructure Network
14 sites

2015-2025
NNCI
National Nanotechnology Coordinated Infrastructure
16 sites

1980 **1990** **2000** **2010** **2020**

Cornell, 1983

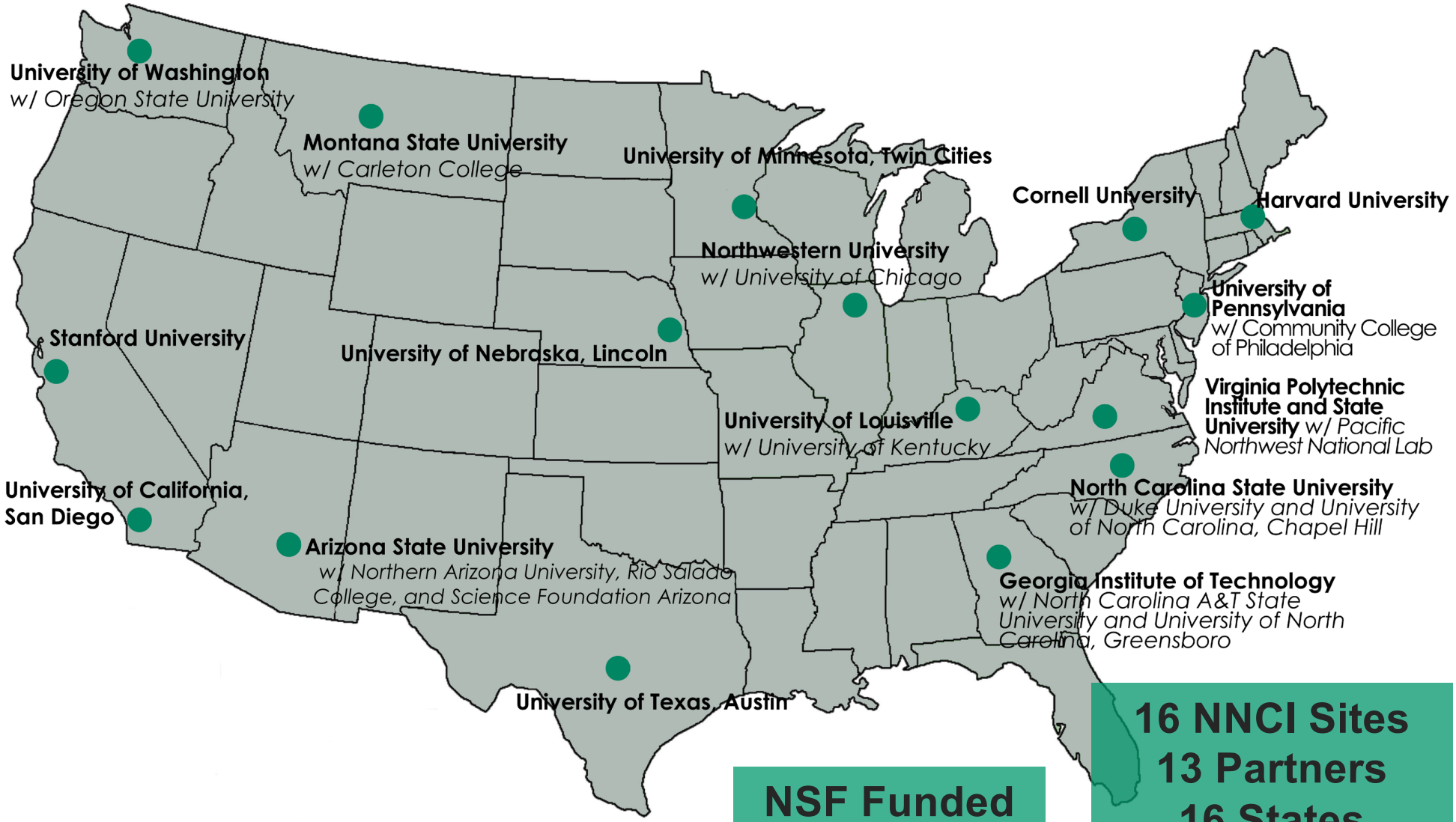
2000 NNI
National Nanotechnology Initiative

2003
21st Century Research and Development Act

U Penn, Singh Center, 2013

National Nanotechnology Coordinated Infrastructure

NNCI Network



NSF Funded
2015 - 2025
$165M total

16 NNCI Sites
13 Partners
16 States
71 Facilities
>2,200 Tools

National Nanotechnology Coordinated Infrastructure

NNCI Goals

- Provide open access to **state-of-the-art nano-fabrication & characterization facilities** and their tools across US and **staff expertise**
- Use these resources to support **education & outreach (E&O)** as well as **societal & ethical implications (SEI)** in/of nanotechnology
- **Network approach to make whole more than the sum of its parts**

National Nanotechnology Coordinated Infrastructure

NNCI by the Numbers

	NNCI Year 6 10/2020 – 09/2021
Unique Facility Users	11,242
Unique External Users	2,793 (24.8%)
Average Monthly Users	4,381
New Users Trained	4,414
Facility Hours	967,297
External Facilities Hours	242,926 (25.1%)

External users represent:

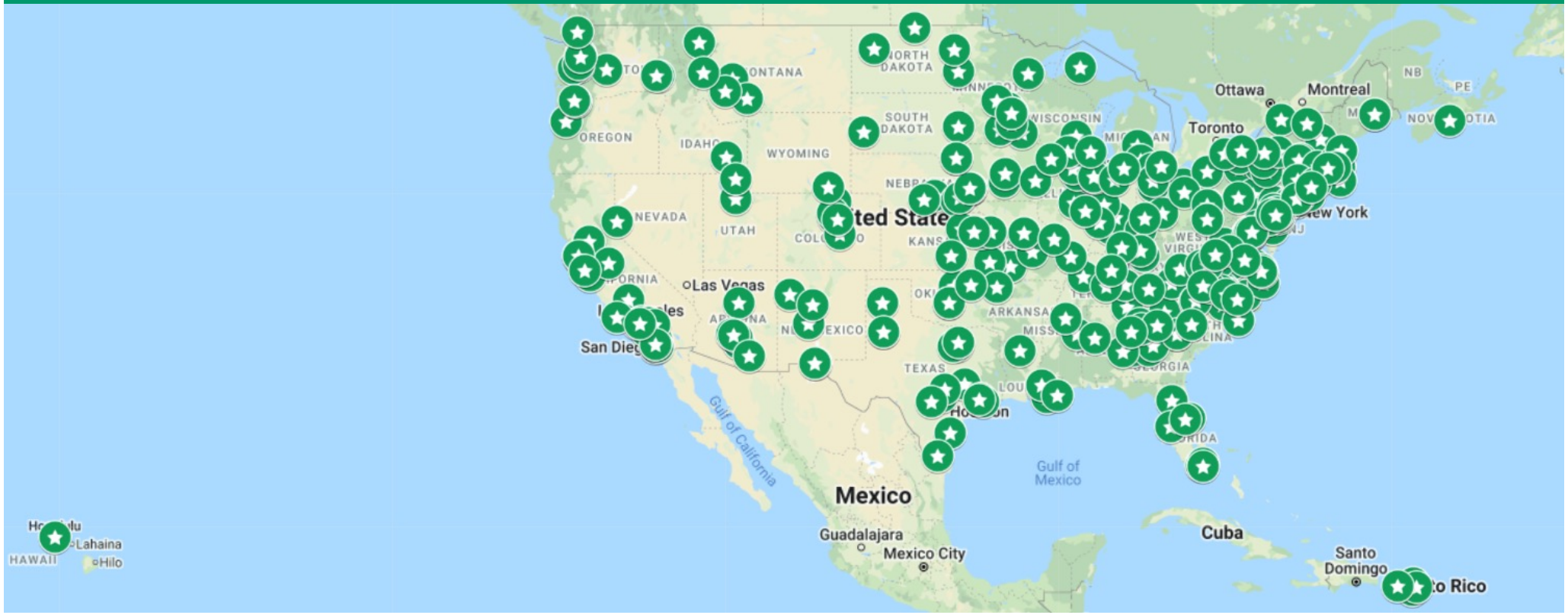
- **198 academic institutions**
- **521 small companies**
- **184 large companies**
- **24 government organizations**
- **39 international institutions**
- **12 other institutions (e.g. museums)**

National Nanotechnology Coordinated Infrastructure

NNCI Year 6 US Academic Institutions (198)

National Nanotechnology Coordinated Infrastructure

NNCI Years 1-5 US Academic Inst. (370)



- Located in 49 states (all but Alaska) plus Puerto Rico
- 131 of the 146 (90%) R1 institutions
- 65 of the 133 (49%) R2 institutions
- 174 (47%) non-R1/R2 institutions
- 76 (21%) serving under-represented populations

National Nanotechnology Coordinated Infrastructure

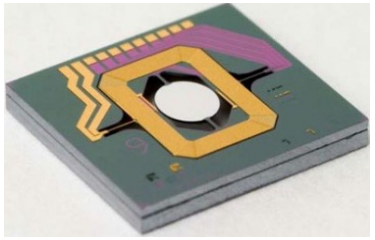
NNCI Resources

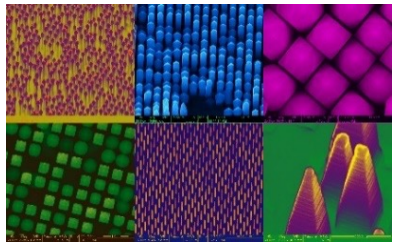
- **Micro- and Nano-Scale Fabrication and Characterization Facilities**
  - Nanomaterials
  - **Electronics**
  - Photonics and Optics
  - MEMS/NEMS
  - Chemistry and Physics
  - Medicine and Life Sciences
  - Geology and Earth Sciences
- Computation and Modeling Capabilities
- Resources and Events for Education and Outreach
- Social and Ethical Implications Activities
- Innovation & Entrepreneurship Activities

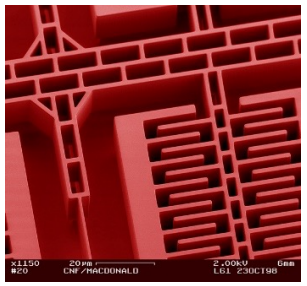
National Nanotechnology Coordinated Infrastructure

NNCI Nanofabrication & Characterization

- Ability to deposit and structure a wide variety of materials, incl. metals, semiconductors, dielectrics, soft materials
- Top-Down (Lithography Defined) Nanofabrication
  - Material Deposition & Growth
  - Lithography (optical and electron-beam)
  - Etching
- Bottom-Up (Synthesis Based) Nanofabrication
- Nanoscale Imaging and Surface Metrology
- **Additive/Subtractive Manufacturing**







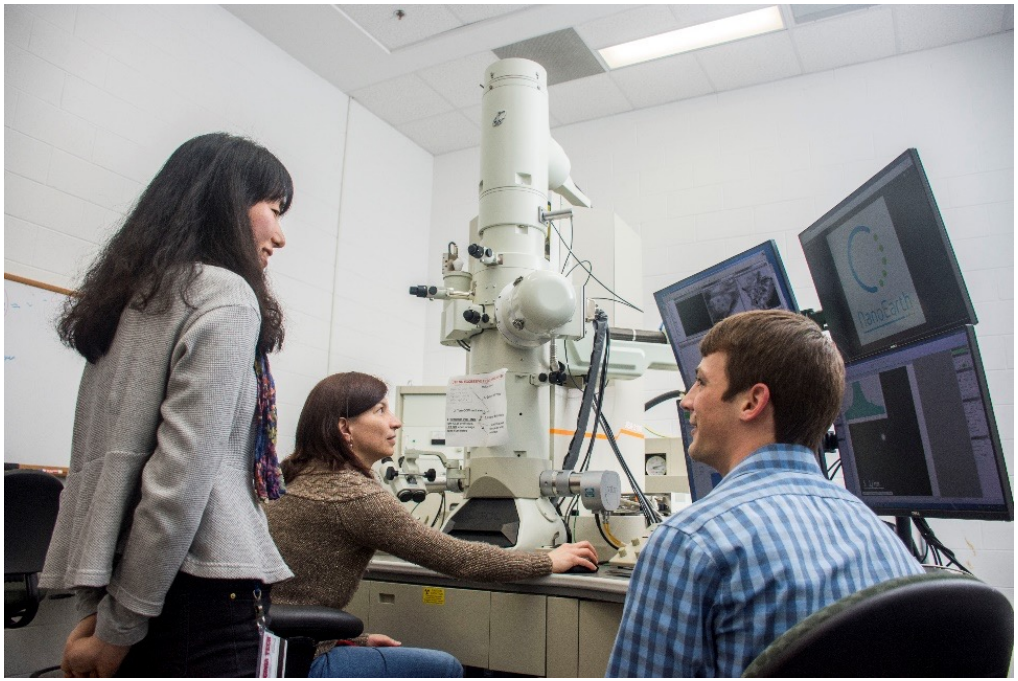
Tool Data Base: https://www.nnci.net/search/tools

Expert Data Base: https://www.nnci.net/search/experts

National Nanotechnology Coordinated Infrastructure

How to Become an NNCI User?

- User access handled by individual sites
- Easy access with academic rates available
- Minimal or no proposal with rolling application
- On-site or remote access
- Seed grants available



Visit https://www.nnci.net/becoming-user for Details

For inquiries Contact Local Site Directly or Complete On-Line Form

National Nanotechnology Coordinated Infrastructure

NNCI Educates

- Offer **hands-on education and training** to address the growing need for a **skilled workforce**
- Provide resources, programs, and materials to **enhance knowledge of nanotechnology** and its application to real-world issues
- Annually, the NNCI impacts **30,000+ individuals** through classroom visits, teacher workshops, remote sessions, short courses, seminars, community events, contacts made at booths at conferences, tours, internships, **REUs**, and RETs. (Online connections are above and beyond this number.)

National Nanotechnology Coordinated Infrastructure

NSF

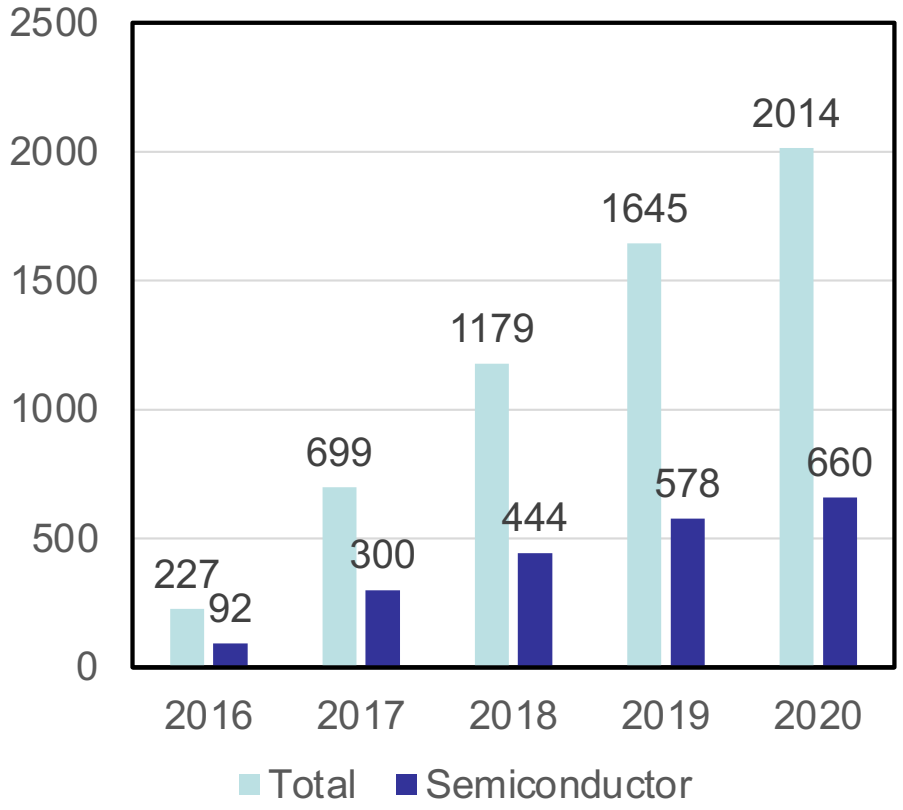
NNCI Research Communities
https://nnci.net/research-communities

- **Research Communities** are organized around a particular research topic, national priority, or grand challenge
  1. Nanotechnology Convergence
  2. Nanoscience in the Earth & Environmental Sciences
  3. Nano-Enabled Internet of Things (August 16, 2022)
  4. Transform Quantum
  5. Understanding Rules of Life
  6. **Microelectronics – Semiconductors (Sept. 8-9, 2022)**
- Serve as **networking opportunities** and provide an **external facing NNCI component**
  - What infrastructure capabilities are needed to support the topic?
  - What are the challenges of current fabrication infrastructure for the specific research area?

National Nanotechnology Coordinated Infrastructure

NNCI and Microelectronics Research

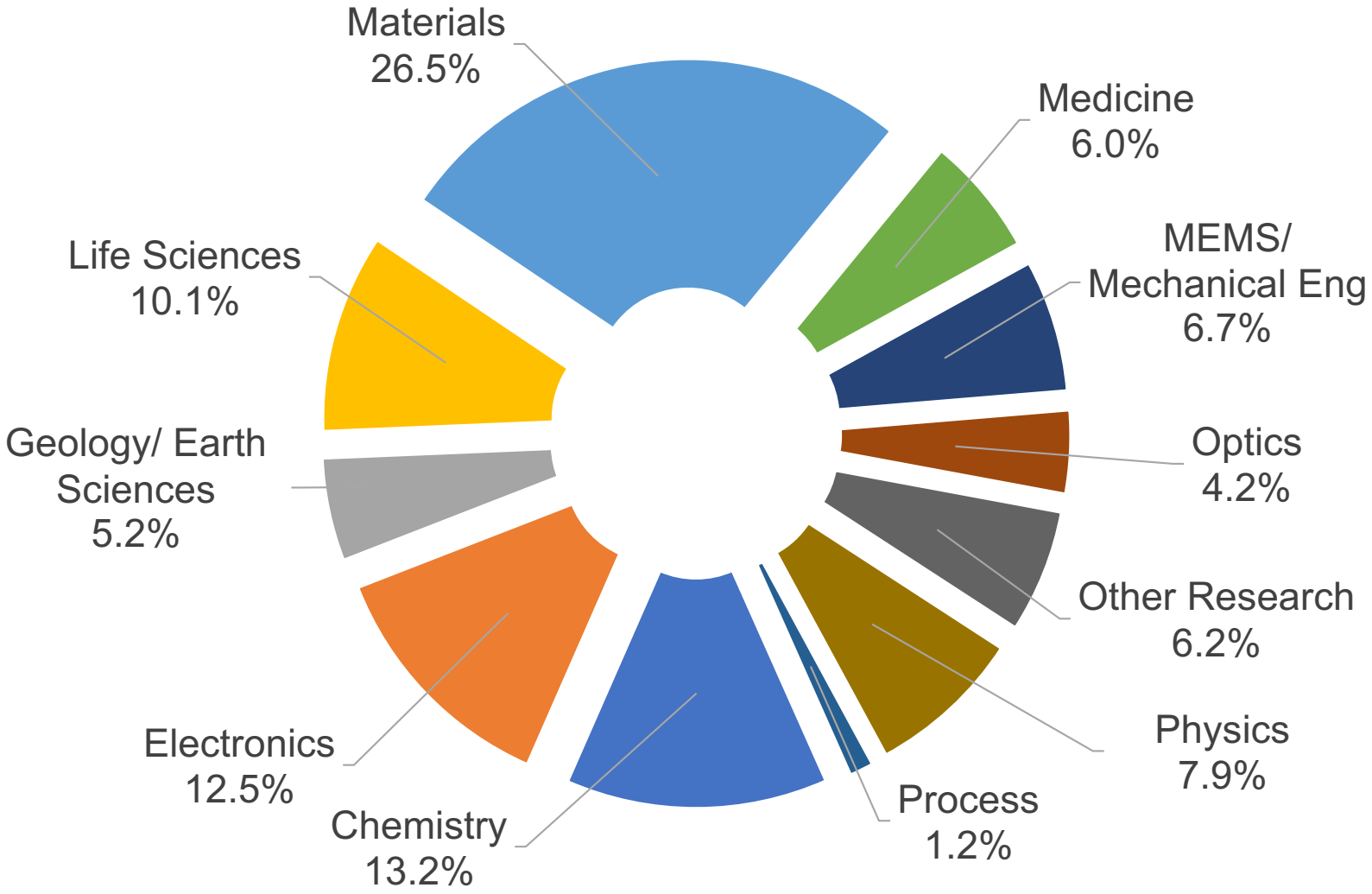
- NSF-funded micro & nanotechnology infrastructure programs have supported microelectronics research for 40+ years
- About one-third of publications referencing NNCI awards contain the search term “semiconductor”
- NNCI facilities train thousands of graduate students every year and reach out to 10-thousands of potential future students
- NNCI facilities are heavily used by start-ups, small and large companies
- NNCI facilities invested $156M in new 600+ new tools over the first 4 years (only 1% was funded using NNCI award $)



*Total number of **annual publications** citing NNCI awards as well as subset including the search term “semiconductor” based on Google Scholar search on March 8, 2021*

National Nanotechnology Coordinated Infrastructure

NNCI Users by Discipline



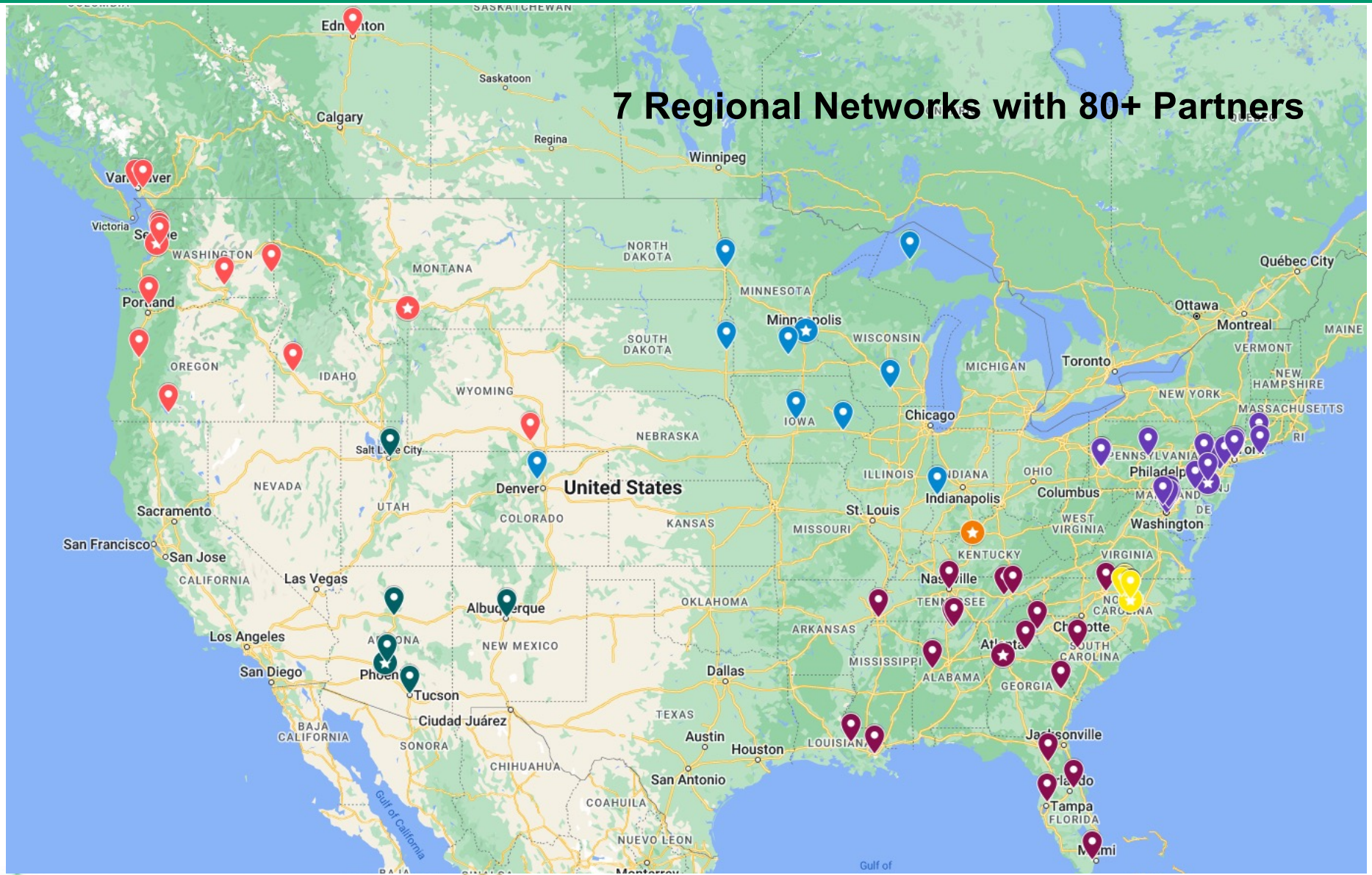
National Nanotechnology Coordinated Infrastructure

Academic Infrastructure Strengths

- **Academic infrastructure is flexible**
  - Low-cost, open access to semiconductor tools and staff expertise
  - Ideal to try out new ideas using new materials, devices, process modules
  - Supports fundamental and applied research
  - 100-150mm infrastructure is cost-effective for research
  - Supports microelectronics PLUS: MEMS; photonics; quantum; wide-bandgap semiconductors; heterogeneous integration; 2D electronics; bioelectronics; flexible electronics; ……
- **Academic infrastructure educates**
  - NNCI hands-on trains 4,000-5,000 new users per year; this could be scaled via regional networks; collaboration with community colleges, etc.
  - Academic infrastructure can excite the next generation via K-12 outreach
- **Academic infrastructure brings people together**
  - Campus locations bring together academicians, start-ups, small & large companies, and even investors
  - Enhanced by workshops, short courses, seminars, tech showcases, etc.

National Nanotechnology Coordinated Infrastructure

Regional Nanotechnology Networks
https://nnci.net/regional-networks



National Nanotechnology Coordinated Infrastructure

Academic Infrastructure Challenges

- **Aging cleanroom infrastructure**
  - Many tools are 10-20+ years old, not vendor supported anymore, and not industry standard
  - Most academic facilities have limited 200mm plus capabilities
  - **Need to invest into upgrading toolsets**
- **Staffing**
  - University salary structure makes it difficult to retain staff
  - Staffing (and tool) cost are sometimes overlooked when building a new academic nanotechnology facility
  - **Need to invest into staff**
- **Limited possibilities to support translational activities**
  - ”Open” vs. “controlled” tools; limited “standard” processes
  - **Need for controlled process modules**
  - **Need to bridge the gap between research & manufacturing**

National Nanotechnology Coordinated Infrastructure

Takeaways

- Utilize/leverage existing facilities and invest in
  - Evergreen research infrastructure (replace aging toolsets)
  - Staff, staff, staff
  - Bridging the gap between basic research and manufacturing
    - Support process modules that researchers can build upon
    - Support more translational activities
- Utilize infrastructure to develop the workforce
  - Hands-on user training
  - Teaching cleanrooms for hands-on class support, short courses
  - Internships, apprenticeships, co-op programs, partnerships with community colleges
  - Pipeline development through K-12 outreach

Need more Information?

http://www.nnci.net

Reasserting U.S. Leadership in Microelectronics and the Role of Universities

– Academic Infrastructure –

Jesús A. del Alamo

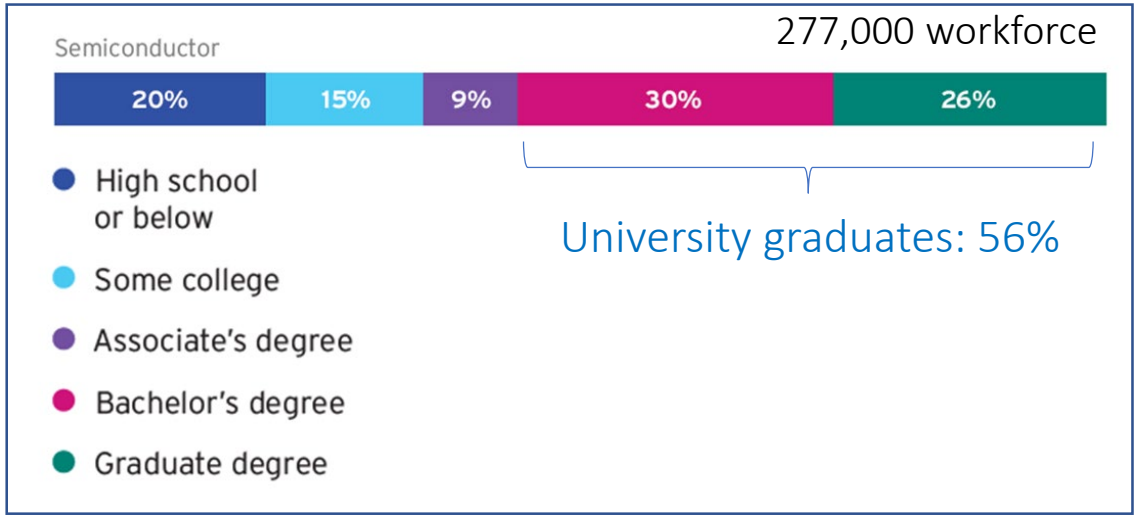
MIT

Microelectronics/Semiconductor Research Community Virtual Workshop

September 8-9, 2022

Universities:
integral element of microelectronics ecosystem

- Contribute >half of microelectronics workforce
- Make new discoveries and invent new technologies
- Facilitate technology translation through startups, graduates, licensing



SIA – Oxford Economics 2021

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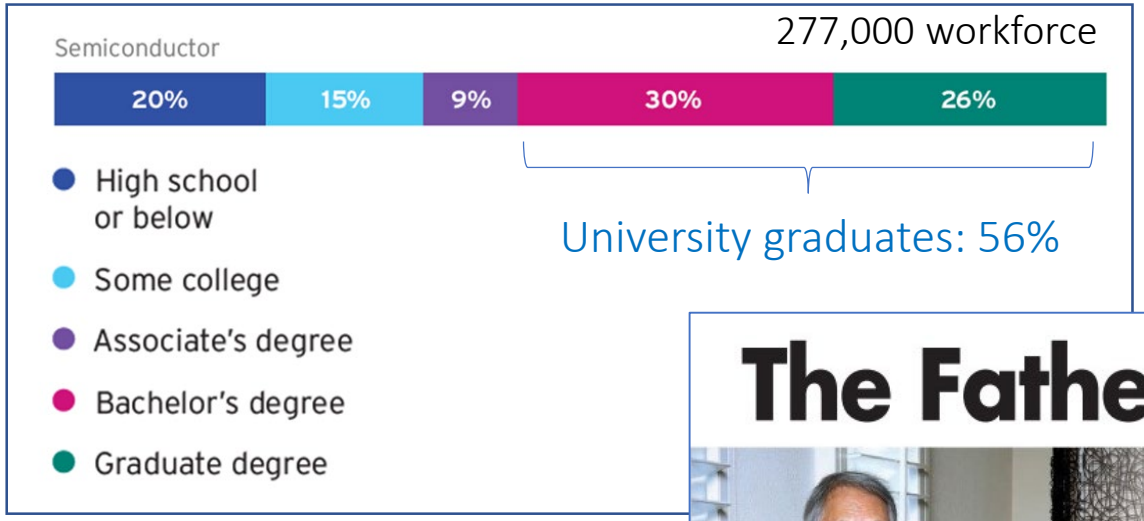

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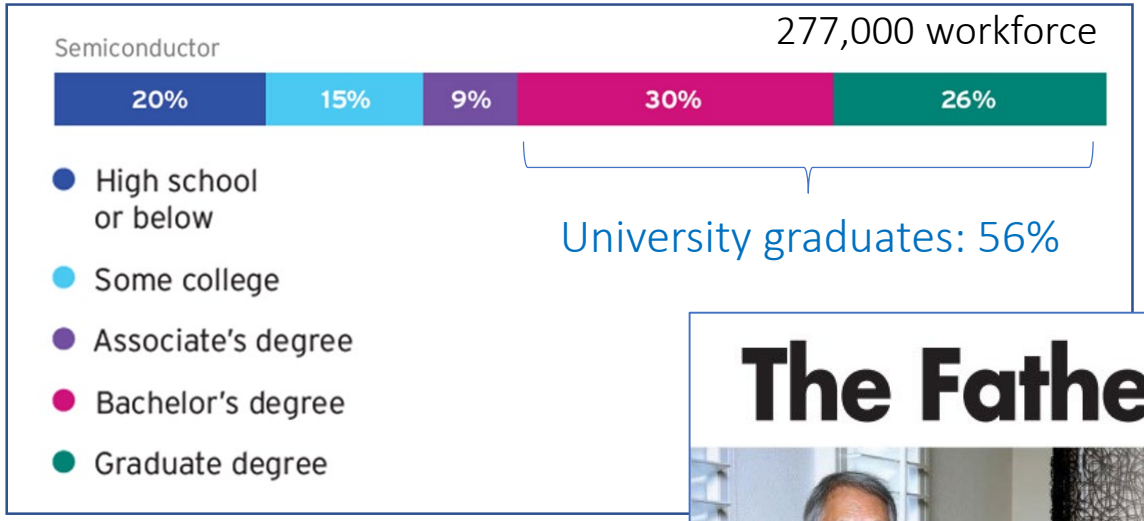
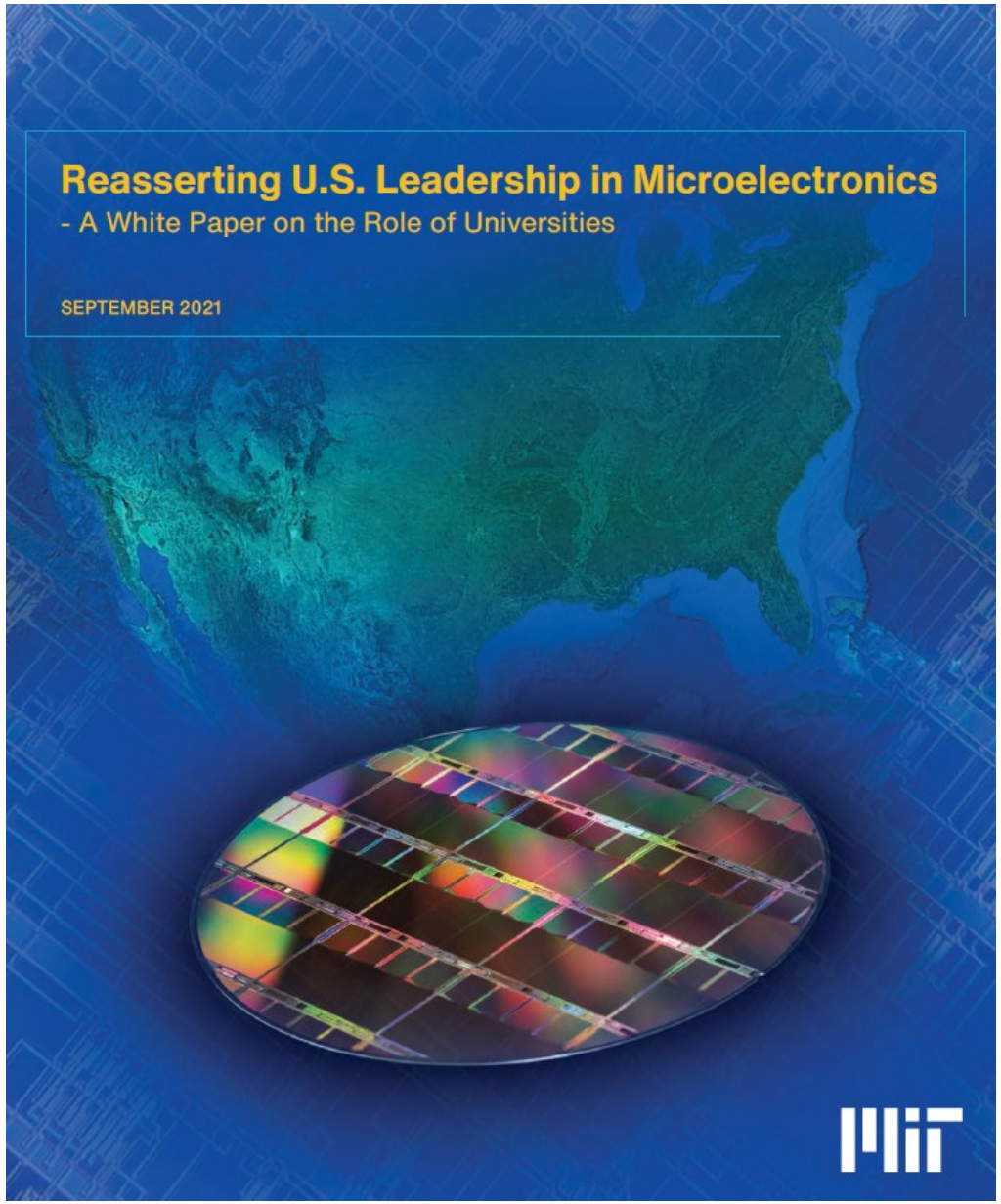


SIA – Oxford Economics 2021

2020 IEEE Awards

http://usmicroelectronics.mit.edu/



Endorsed by 50 colleagues at 32 universities

Reasserting U.S. Leadership in Microelectronics

- A White Paper on the Role of Universities

- Executive Summary
- U.S. leadership in microelectronics
- Education and workforce development
- Research
- Technology translation, startups and intellectual property
- Academic infrastructure
- Regional network efficiencies
- Appendix A: 200 mm: the “sweet spot” for industry-relevant microelectronics research in universities

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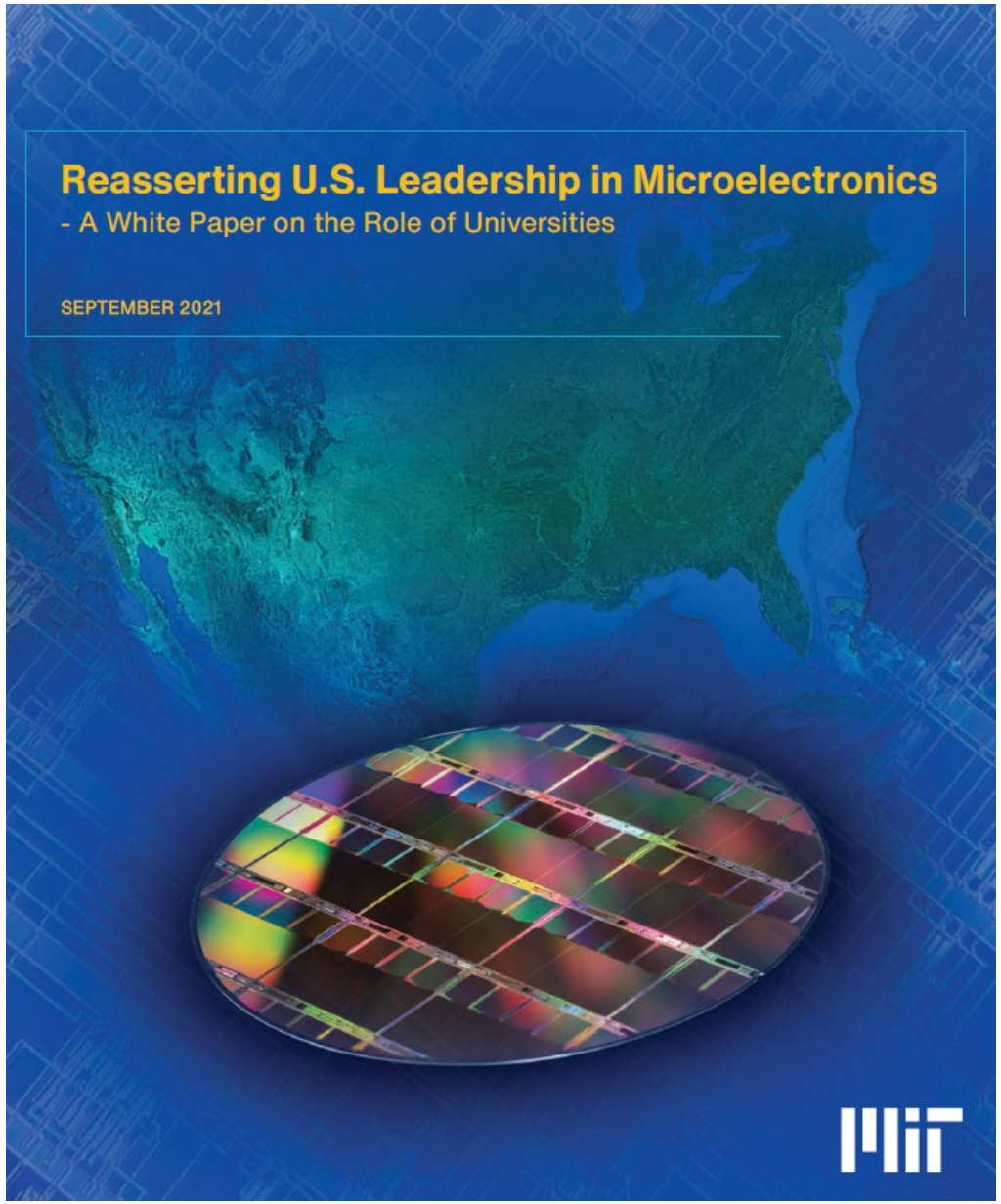

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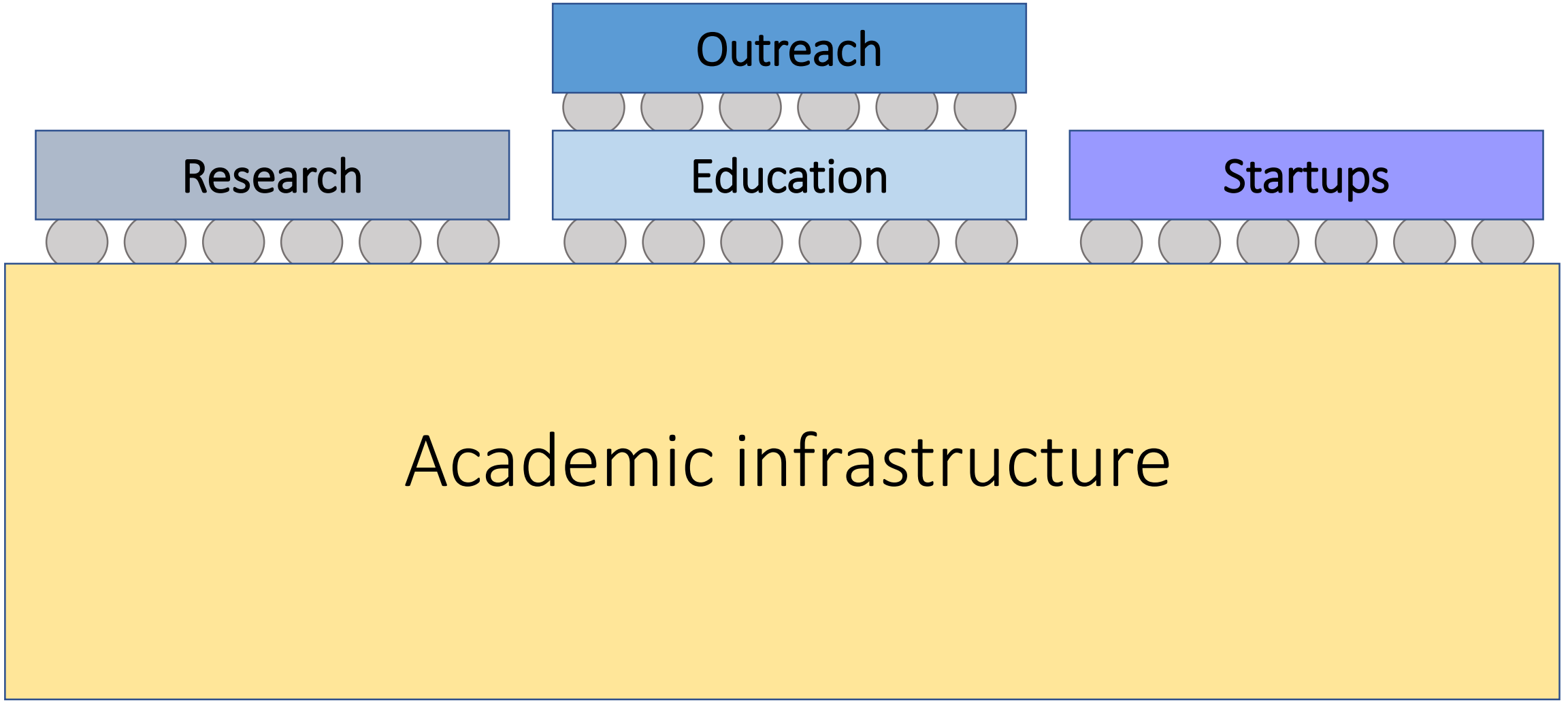
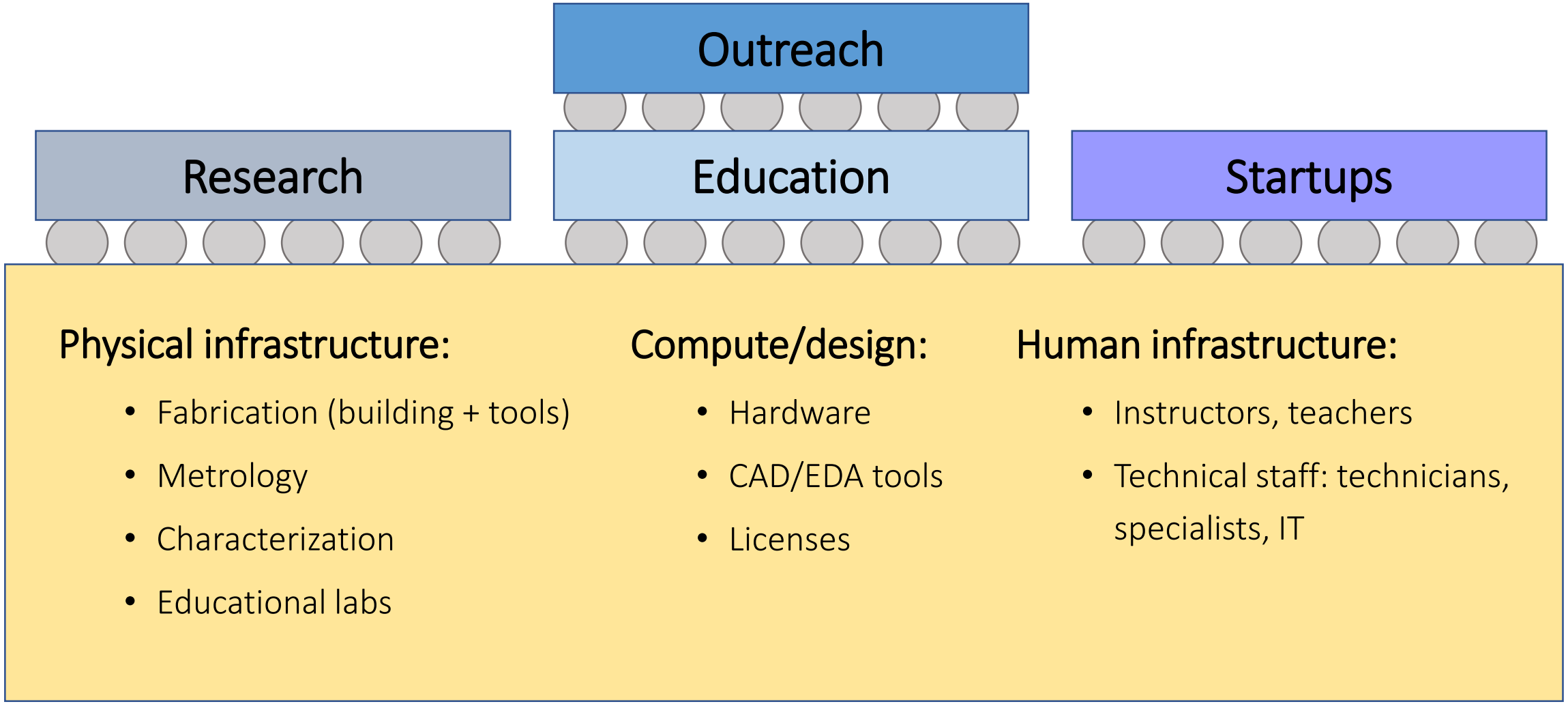
- Appendix A: 200 mm: the "sweet spot" for industry-relevant microelectronics research in universities

Authors: Jesús A. del Alamo, Dimitri A. Antoniadis, Robert G. Atkins, Marc A. Baldo, Vladimir Bulović, Mark A. Gouker, Craig L. Keast, Hae-Seung Lee, William D. Oliver, Tomás Palacios, Max M. Shulaker, Carl V. Thompson


Outreach
Research
Education
Startups
Academic infrastructure


Outreach
Research
Education
Startups
Physical infrastructure:
• Fabrication (building + tools)
• Metrology
• Characterization
• Educational labs
Compute/design:
• Hardware
• CAD/EDA tools
• Licenses
Human infrastructure:
• Instructors, teachers
• Technical staff: technicians, specialists, IT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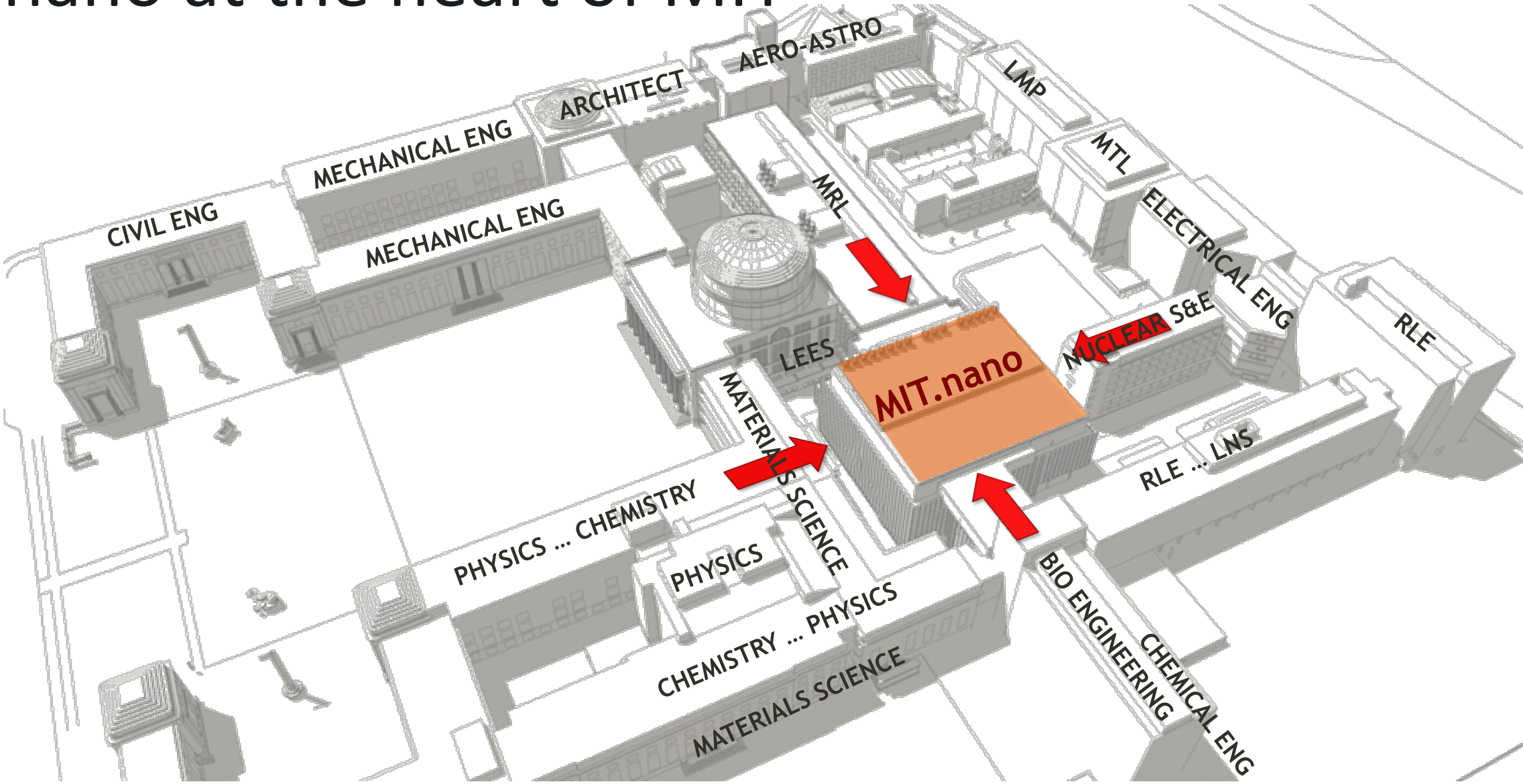
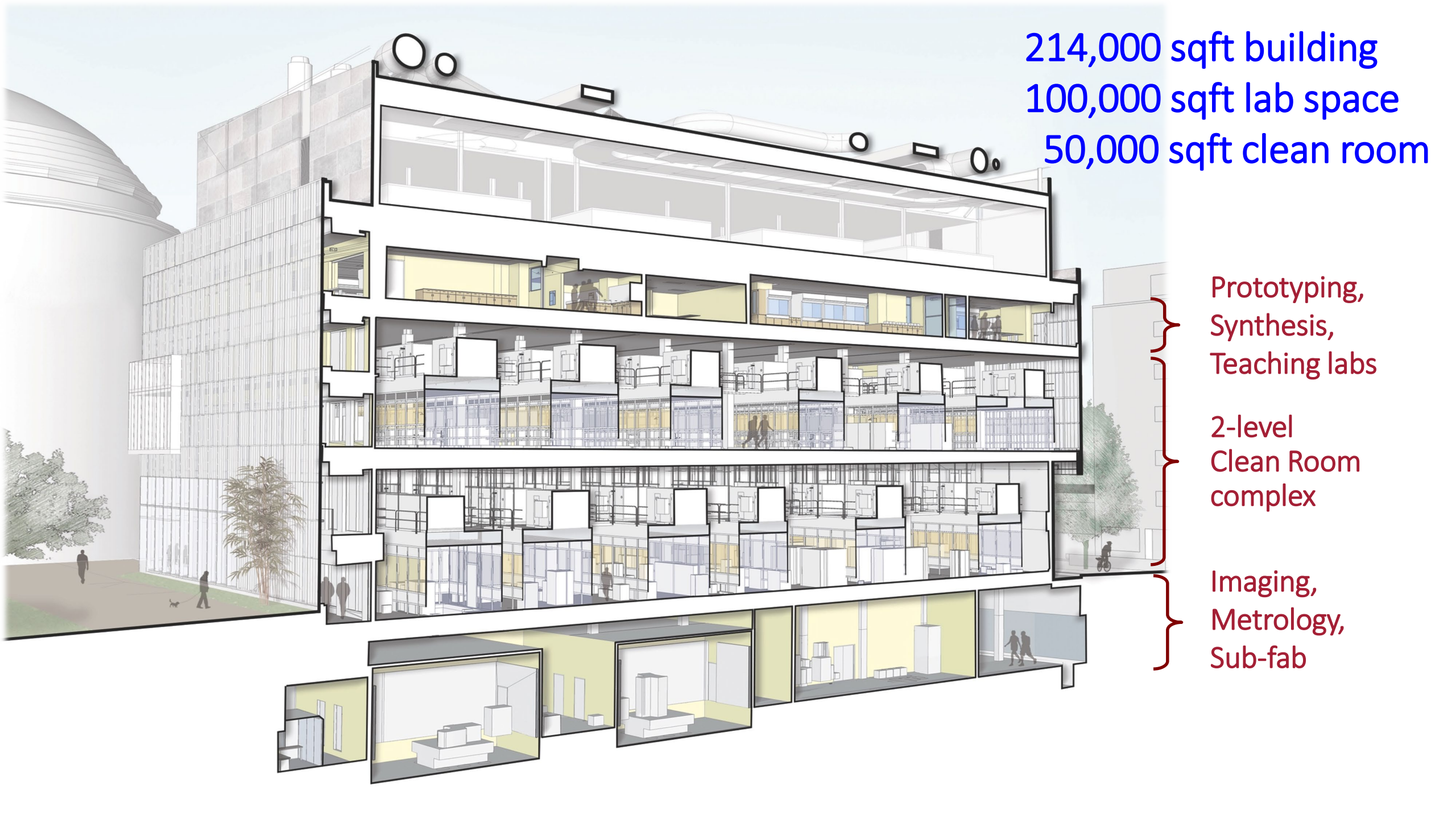
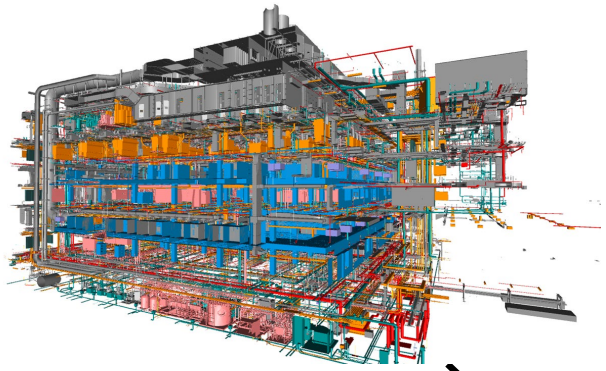
@
Lisa T. Su Building

MIT.nano at the heart of MIT



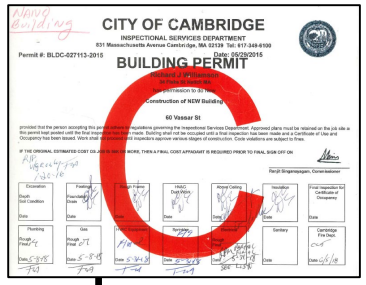

214,000 sqft building
100,000 sqft lab space
50,000 sqft clean room
Prototyping,
Synthesis,
Teaching labs
2-level
Clean Room
complex
Imaging,
Metrology,
Sub-fab

MIT.nano: a 10+ year endeavor!



Bldg. 12 demolition

Certificate of Occupancy



Building dedication

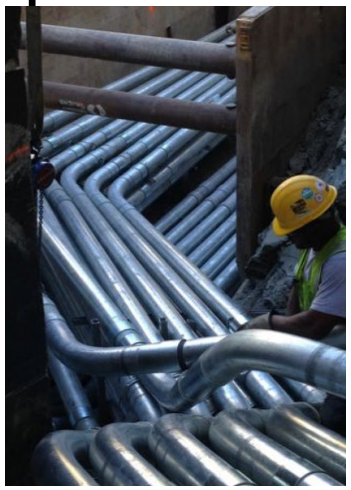
Planning | Design | Construction | Tool hookup + Operation

2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

Bldg. 39 fab, since 1985

MIT Corporation approval

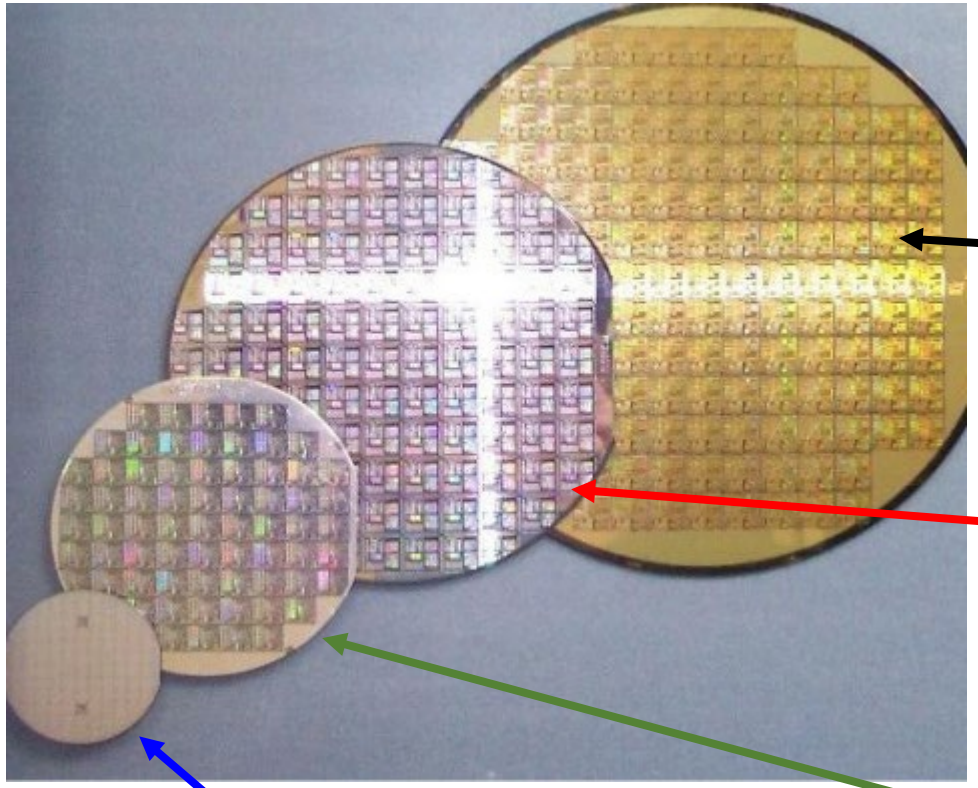
Facilities prep completed



Inauguration

Bldg. 39 fab decommissioned

Wafer landscape



450 mm (uncertain future)

300 mm (~2000):
CMOS, CMOS+, memory

200 mm (~1990):
legacy CMOS, MEMS, smart power, image sensors, analog, RF, LEDs, mmw, GaAs, GaN, SiC

150 mm (~1980):
GaN, SiC, InP

Economics of university fab

Annual fab maintenance + staffing cost ≈ Annual fab fees

Cannot use fab fees to buy new fab tools

Economics of university fab

Annual fab maintenance + staffing cost ≈ Annual fab fees

Cannot use fab fees to buy new fab tools

"

Tool suite investment x 0.2

Annual maintenance and staffing cost: ~20% of tool cost

Economics of university fab

Annual fab maintenance + staffing cost ≈ Annual fab fees

Cannot use fab fees to buy new fab tools

〃 〃

Tool suite investment x 0.2 ≈ Annual research volume x 0.2

Annual maintenance and staffing cost: ~20% of tool cost

Research contracts can at most dedicate 20% of budget for fab fees

Economics of university fab

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Tool suite investment ≈ Annual research volume

Economics of university fab

Tool suite investment ≈ Annual research volume

Annual research volume ≈ # Users x $150K

Typical research contract: 1 student/postdoc at ~$150k/yr
→ $30K for fab fees

Economics of university fab

Tool suite investment ≈ Annual research volume

Annual research volume ≈ # Users x $150K

Typical research contract: 1 student/postdoc at ~$150k/yr → $30K for fab fees

$$\#\ \text{Users} \approx \frac{\text{Tool suite investment}}{\$150\text{K}}$$

Economics of university fab vs. wafer diameter

Tool suite investment ≈ Annual research volume

$$\#\ \text{Users} \approx \frac{\text{Tool suite investment}}{\$150\text{K}}$$

TOOL SUITE WITH WAFER DIAMETER OF:	COST OF OBTAINING TOOL SUITE (LITHO/DEPOSITION/ ETCHING)	ANNUAL COST OF TOOL MAINTENANCE & STAFFING (20% TOOL COST)	ANNUAL RESEARCH BASE (5X MAINTENANCE & STAFFING COSTS)	#PHD/MASTER'S/ POSTDOCS
150 mm	$15M	$3M	$15M	100
200 mm	$80M	$16M	$80M	533
300 mm	$500M	$100M	$500M	3,333

Economics of university fab vs. wafer diameter

Tool suite investment ≈ Annual research volume

$$\#\ \text{Users} \approx \frac{\text{Tool suite investment}}{\$150\text{K}}$$

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Inconceivable!

Economics of university fab vs. wafer diameter

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Eminently feasible: the "sweet spot"!

Inconceivable!

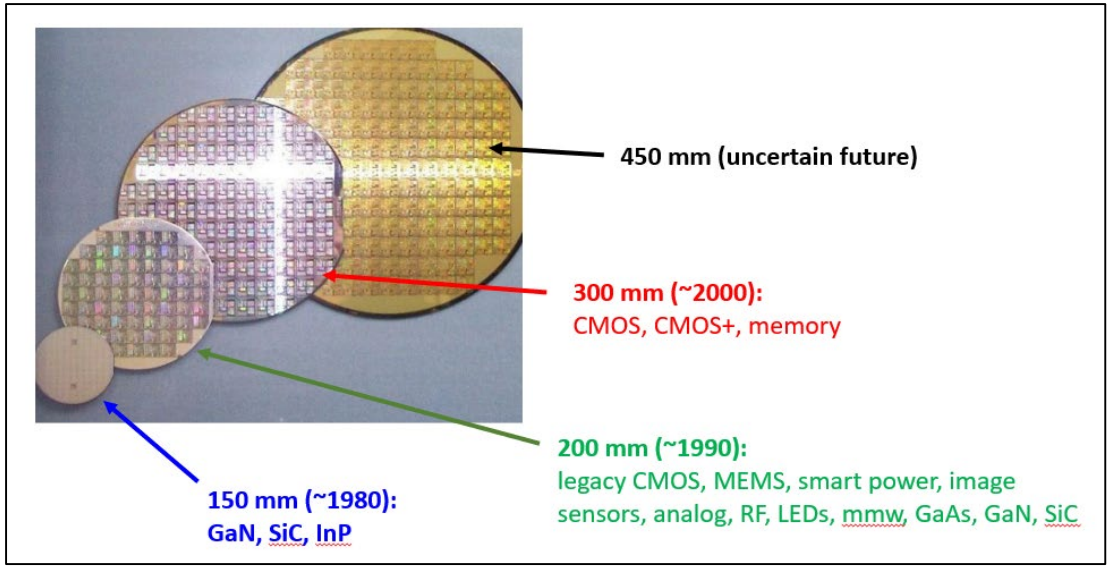
533 ≈ 4% of # MIT grad students + postdocs

$80M ≈ 11% of MIT campus research volume

8 insights from

white paper study and fab economics

Insight #1:
200 mm: the "sweet spot" for *industry-relevant* microelectronics research at universities



- Supports research over very wide intellectual front, enables collaborations with industry and national labs
- High-performance tools
- Thriving 200 mm tool market with spare parts, maintenance contracts available
- Effective in industry-relevant education and workforce development
- No US university hosts a well equipped 200 mm tool line

Insight #2:
Toolset must be broadly shared

- Across wafer sizes and sample shapes
- Across materials
- Across processes
- Across device types, disciplines
- In research, education, outreach and startup support
- Inside and outside the institution including industry

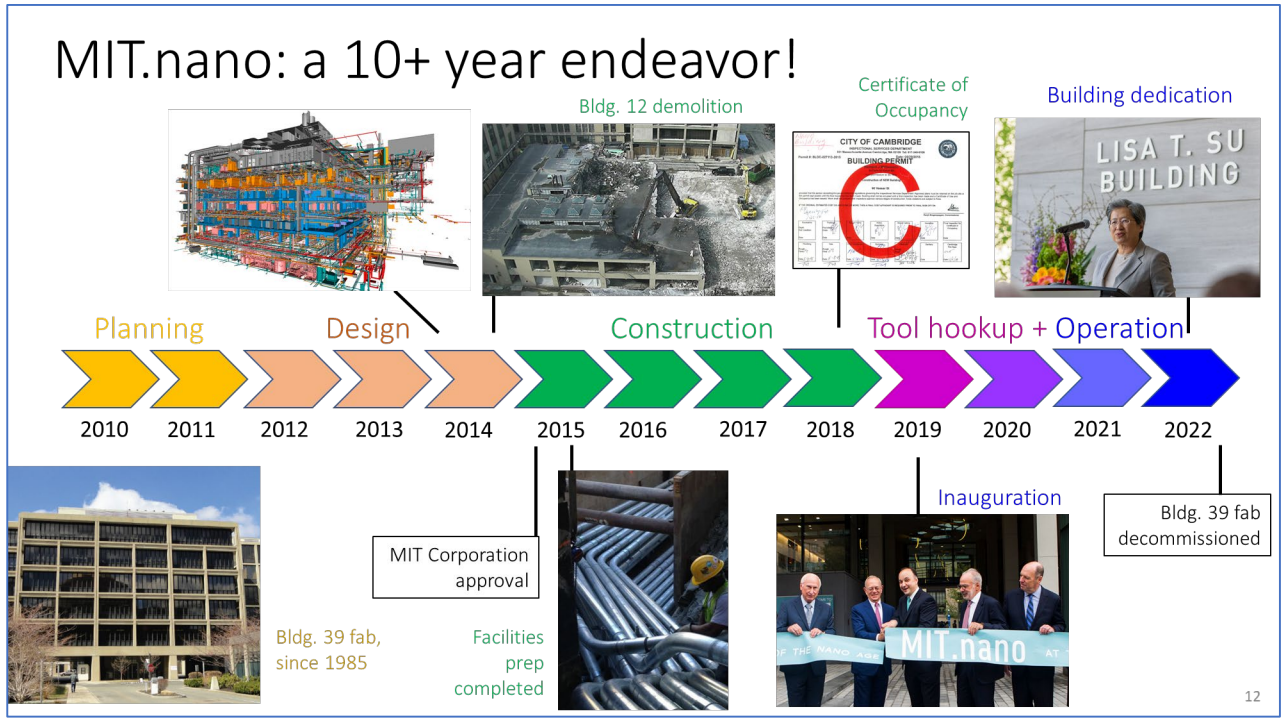
Insight #3 (Principle of “detailed balance”!): Infrastructure investments and research volume must be balanced *in detail*

- Infrastructure investments must go hand-in-hand with adequate research volume
- Efficient use of investments
- Long-term sustainability of operations
- Also across programs: NSTC, NAPMP, NNMRD, NSF

Tool suite investment ≈ Annual research volume

Insight #4:
Leverage existing facilities

- Long process for planning/design/construction/commissioning of new facility
- 200 mm tools large and complex: difficult to host in retrofitted facilities



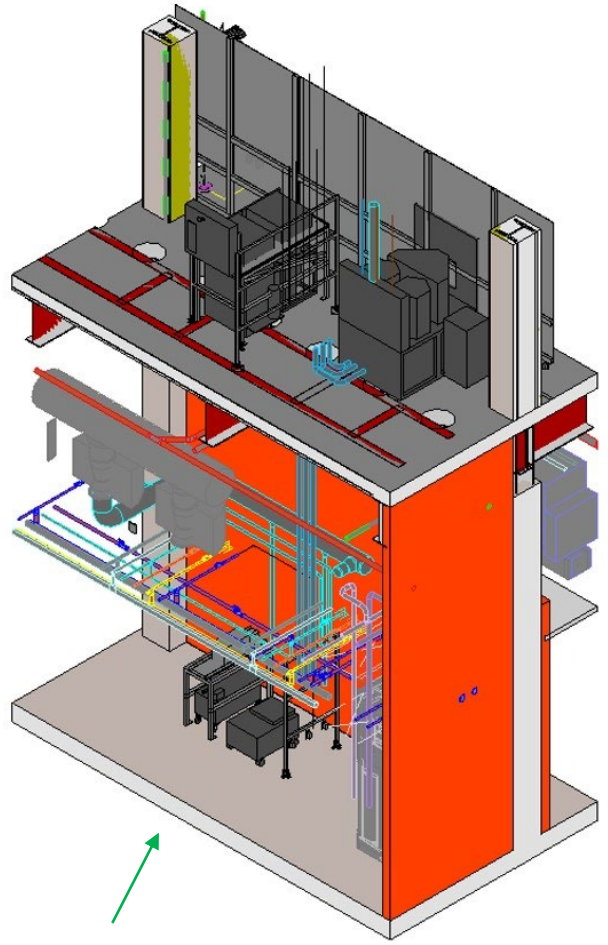
Insight #5:
Tool donations helpful but insufficient

- Spotty coverage of processing capabilities
- For 200 mm cluster tools, need subfab, expensive installation costs!

Donation of five 200 mm cluster tools under discussion at MIT:

- Tool cost: $20M
- Facility cost: $5M
- Installation cost: $7.5M

How to pay?



MIT.nano subfab

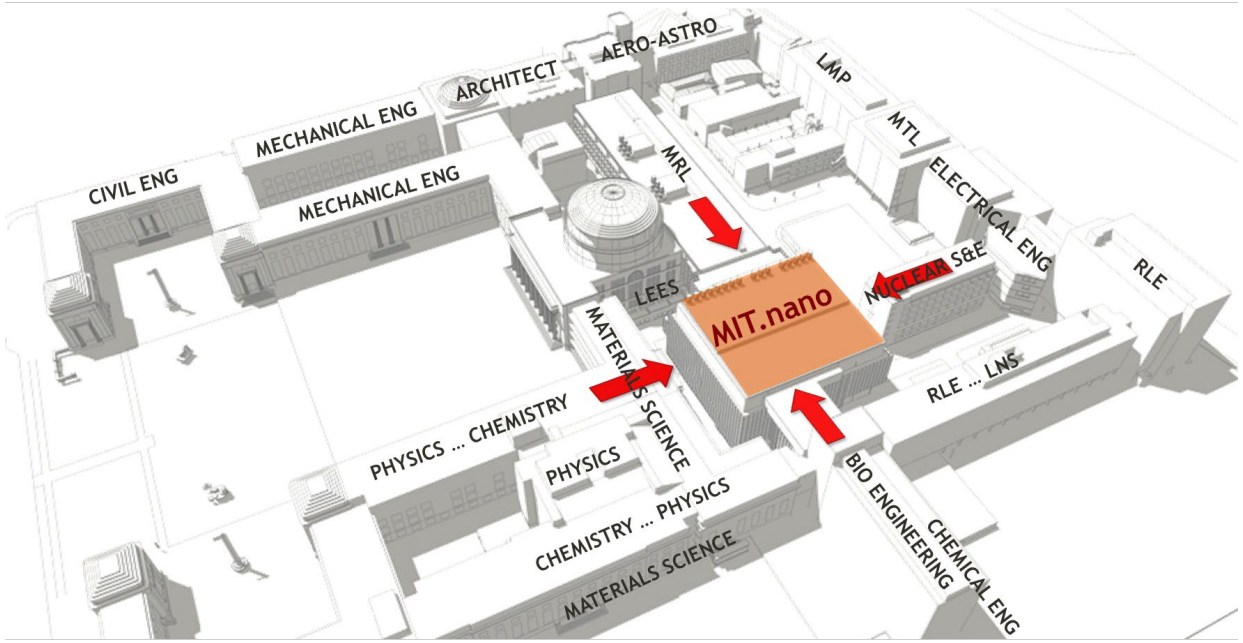
Insight #6:
Must achieve critical mass of capabilities at any one location

- Complex device fabrication involves many process steps engaging different tools
- Process steps are highly interactive
- Need extensive metrology and characterization
- Complex process integration requires reasonably complete tool set at one site

Insight #7:
Need central location on campus

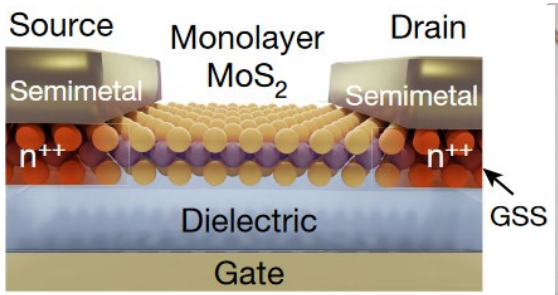
- To be relevant in research, education and outreach at all levels
- More costly, politically difficult, takes longer time than in “green field”

Insight #7b:
Need independent administrative unit that reports to the top

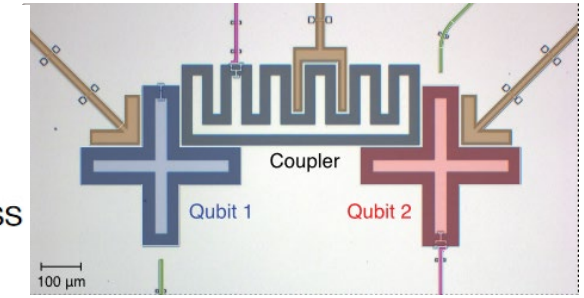


Insight #8:
Think (well) beyond Si!

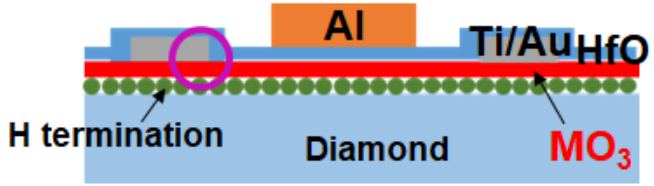
- Microelectronics at a crossroads: future involves new concepts, new material systems, new physics,…
- Need highly flexible tool set that can be broadly shared…
- Yet, it satisfies the mission that brought the tools



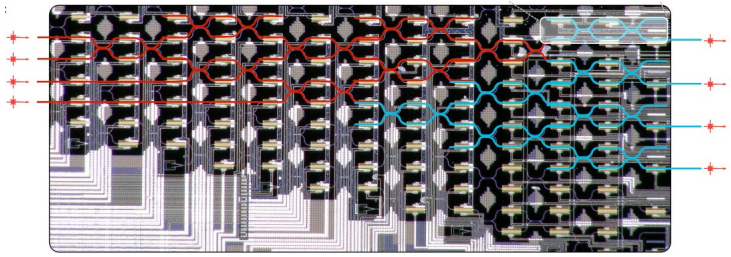
2D MOSFET



Superconducting Qbits

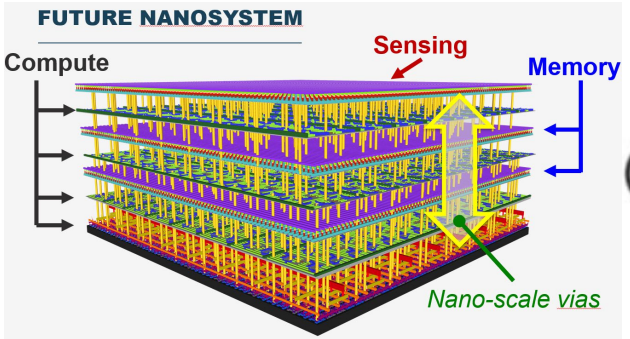


Diamond MOSFET

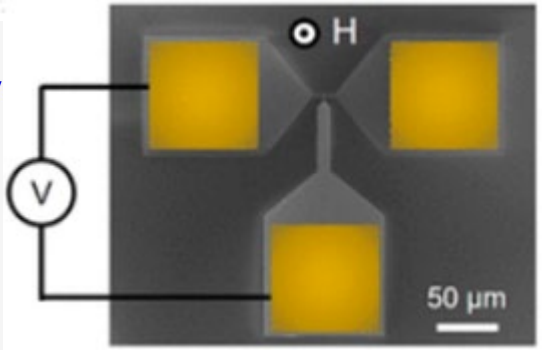


Photonics AI Accelerator

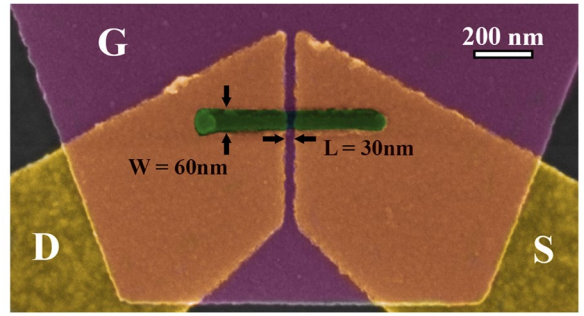
Metallic channel memristors



Monolithic 3D Systems



Magnetic domain wall synapse

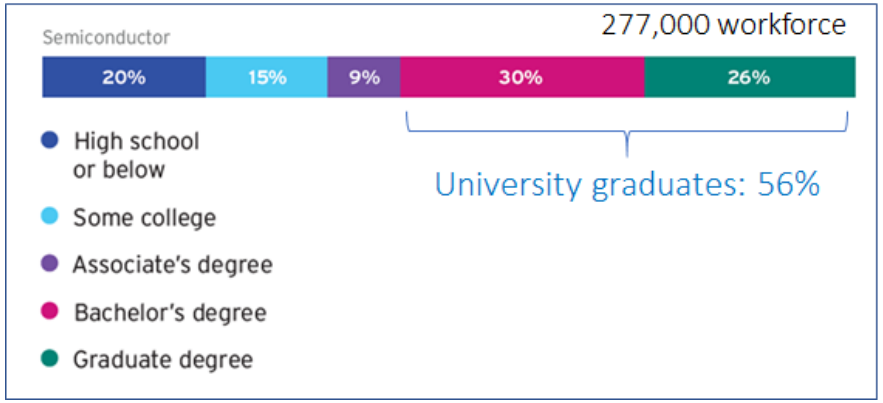


Electrochemical synapse

How to size academic infrastructure investment?

At the minimum, must support development of next generation workforce:

- CHIPS Act: $39B in fab support → ~8 new fabs
- ~27,000 new employees over 10 years
  - ~26% with SM and PhDs → **~7000 new advanced graduates**
  - ~30% SB's → **~8000 new college graduates**



SIA – Oxford Economics 2021

How to size academic infrastructure investment?

Research projects for ~7000 advanced graduates:

- ~3 yr <school residence time>
- ~$150K/yr → $3.2B over 10 years

→ $320M/yr new research program over 10 years

→ **$320M new investment in research tools + 25% installation costs:**

$400M new research infrastructure investment

How to size academic infrastructure investment?

Educational experiences for ~8000 SB graduates:

- Research universities can educate many
  - → need to duplicate heavily used tools (litho, imaging): ~$2M/each
  - → 20 universities: total $40M
- DEI goals require participation of non-mainstream colleges and universities
  - → new education-focused tool sets: $10M/each (assume facility exists)
  - → 10 universities/colleges: total $100M

→ **$140M EWD infrastructure investment + 25% installation costs:**

$175M new education infrastructure investment

Total: $575M new infrastructure investment

Conclusions and recommendations

- US university microelectronics infrastructure obsolete

  → Limited capability to support U.S. Government and industry desires to reassert U.S. semiconductor leadership

- It takes long time to plan, build and bring to full operation a new state-of-the-art university fab

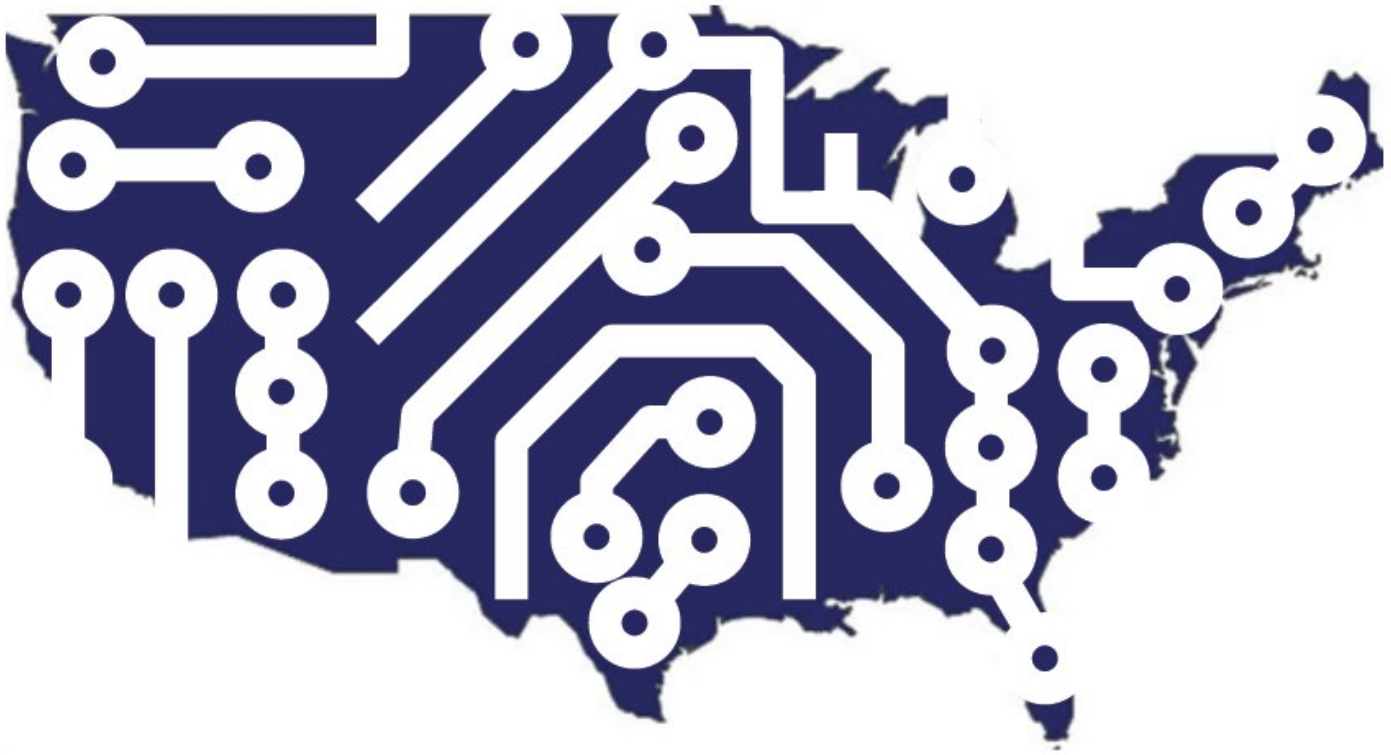
  → for 5 year impact, must heavily leverage existing facilities

- 200 mm: the “sweet spot” for industry-relevant microelectronics research at universities

  → U.S. needs a few 200 mm full-flow university microfabrication facilities… fast!

Conclusions and recommendations

- Must achieve critical mass of capabilities at anyone location
- Need central location on campus
- Very challenging economics of university fabs
  - → Tools must be broadly shared
  - → Think well beyond Si!
  - → Infrastructure investments and research volume must be balanced *in detail*
  - → Tool donations helpful but insufficient
- Accomplishing US Government goals demands >$575M in academic infrastructure investments in the immediate future



http://usmicroelectronics.mit.edu/

Shaping the Future

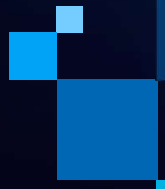
Intel's Academic Collaborations

Gabriela Cruz Thompson

Sowmya Venkataramani

University Research & Collaboration

Intel Labs



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World-changing
Technology
Our Purpose
We create world-changing technology
that enriches the lives of every person on Earth
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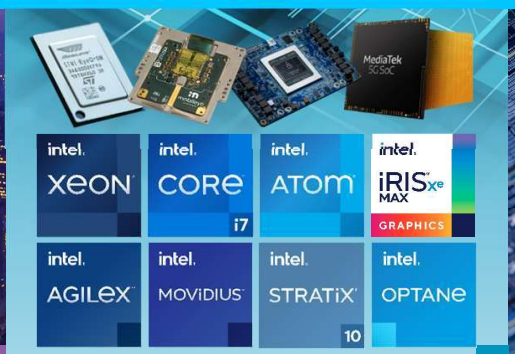
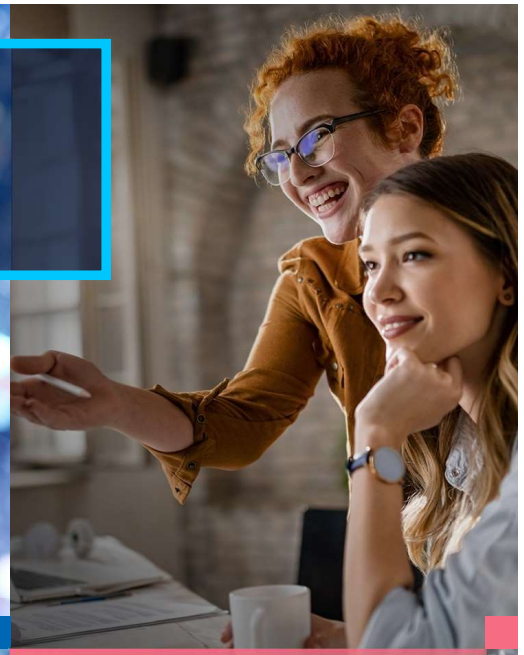
Our Priorities





Innovate with boldness

Lead in every category

Execute flawlessly

Foster vibrant culture

We are positioning Intel for sustained growth and leadership in an increasingly digital world

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"The ingredient we start with is sand.
Everything else is value added by people."

Andy Bryant
Former Intel Chairman

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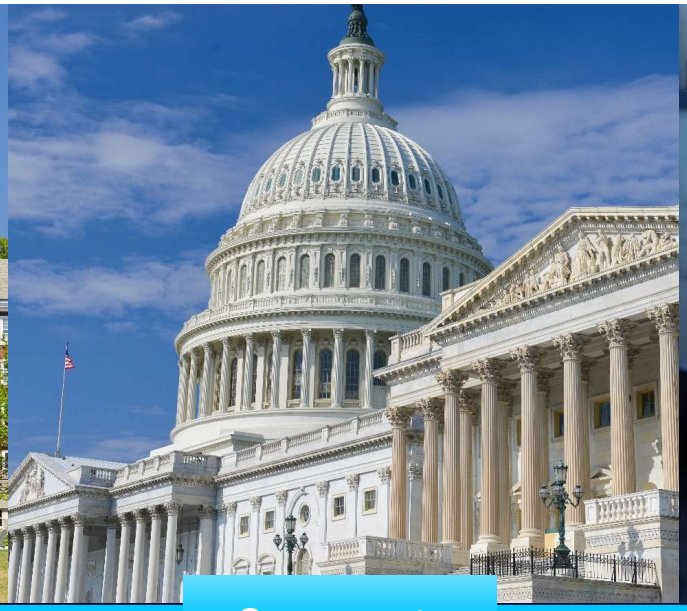
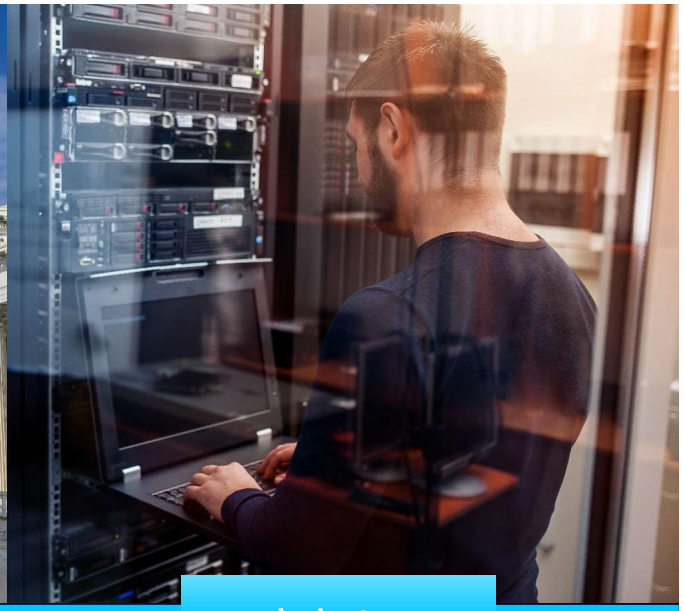
Academia



Governments



Industry

We Seek

Working With Leading Academic, Industry And Government Research Institutions

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Academic Outreach: Mechanisms

SENSE

- Very Large Centers – Semiconductor Research Corp (SRC)
  - DARPA, NIST, NSF and 15 Industry Collaborators
- Large Centers – Government Collaborations
  - NSF

TRANSFER

- Midsize Centers – Research Innovation Pipeline
  - Intel Science and Technology Centers (ISTCs), Intel Collaborative Research Institutes (ICRIs), Intel Strategic Research Alliances (ISRAs)
- Individual Grants – Problem Solving & Business Solutions
  - Strategic Research Sectors (SRS), Memberships/Industrial Affiliations

TALENT

- Intel's Academic Mindshare
  - IA affinity & Community building
- Diversity Higher Education
- Campus Recruiting

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We Solve

Key Research Focus Areas

Trust, Security, & Privacy

- Fully Homomorphic Encryption
- Confidential Computing
- Private AI

Emerging Workloads

- AI - Population Scale Data

Next Wave of AI

- AI for Optimization
- Knowledgeable AI
- Human & AI systems

Future of Software

- NSF PPoSS Machine Programming

Novel Sensing Technologies

- 4D Radar

New Compute Models

- Quantum
- Neuromorphic

Advanced Memory & Storage

Next-gen Connectivity, 5G & Beyond

- Integrated Photonics

Efficient Design & Programming

- Agile HW-SW Co-design

Advancing Manufacturing Leadership

- Beyond CMOS
- Heterogeneous Integ.

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Intel's Mindshare at Universities

Drive Intel's Thought Leadership Into Academia to Foster and Develop a Pipeline of Students' Savvy On Intel Technology and Monitor Technology Inflections

CURRICULUM

Encourage the use of Intel technology in the classroom

STRATEGIC UNIVERSITIES

Continuously connected with key institutions

RECOGNITION AWARDS:

Outstanding Researcher (ORA)

Rising Star (RSA)

Faculty awards recognizing great collaborators and their connection with Intel

ACADEMIC COMPUTE ENVIRONMENT

Cloud computing access to Intel technology for research

UNIVERSITY SHUTTLE PROGRAM

Offer new technologies and products through the IFS in partnership with leading academics

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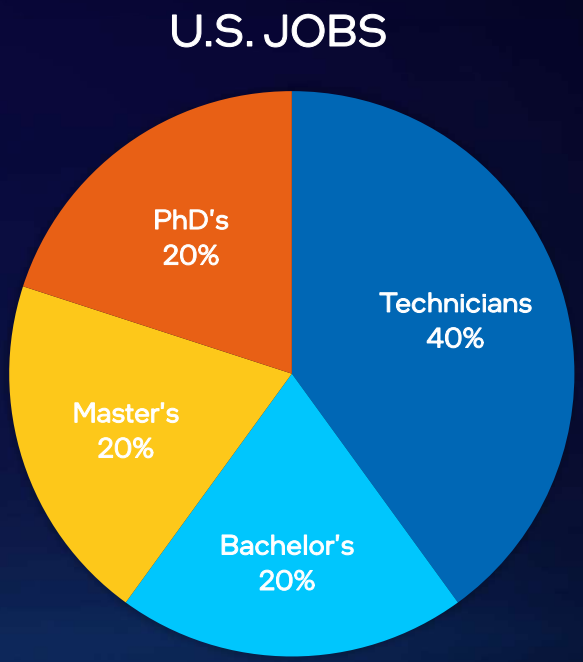
STEM Workforce Needs

CHIPPING IN: THE U.S. SEMICONDUCTOR INDUSTRY WORKFORCE AND HOW FEDERAL INCENTIVES WILL INCREASE DOMESTIC JOBS

SIA/Oxford Economics Report:
Robust federal incentives for domestic chip manufacturing would create an average of nearly 200,000 American jobs annually as fabs are built and add nearly $25 billion annually to U.S. economy



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Intel Jobs New Factories

Job Roles	Education
Manufacturing Technicians	Associates degree Microelectronics, Electronic Engineering Technology, Computer Electronic Engineering Technology. Certifications: Diesel Mechanics, aircraft mechanics, HVAC or relevant work experience
Equipment Technicians	Associate degree in at least one of the following disciplines: Mechanical, Mechatronics, Electrical / Electronic engineering or relevant work experience
Automation Technicians	Associate degree in at least one of the following disciplines: Mechanical, Mechatronics, Electrical / Electronic engineering or relevant work experience
Facilities Technicians	Associate degree in at least one of the following disciplines: Mechanical, Water, Industrial Waste Water, Chemical, Electrical, HVAC or relevant work experience
Process Engineers Equipment engineer	Physics, Materials Science, Electrical Engineering, Chemical Engineering, Mechanical,
Yield Engineers	Physics, Chemistry, Materials Science, Electrical Engineering
Manufacturing Engineer	MFG engineering/Industrial Engineering
Industrial Engineer	Industrial Engineering/MFG engineering
Facilities Engineer	Chemical, Mechanical, Electrical

Other potential opportunities: Research, Manufacturing & Facilities, Software, Hardware, System on a Chip, Silicon Photonics, IT, AI, Sales & Marketing, Business

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Intel Invests $100 Million in Ohio and National Semiconductor Education and Research

$50 Million

$50 Million + **$50** Million Match

NSF

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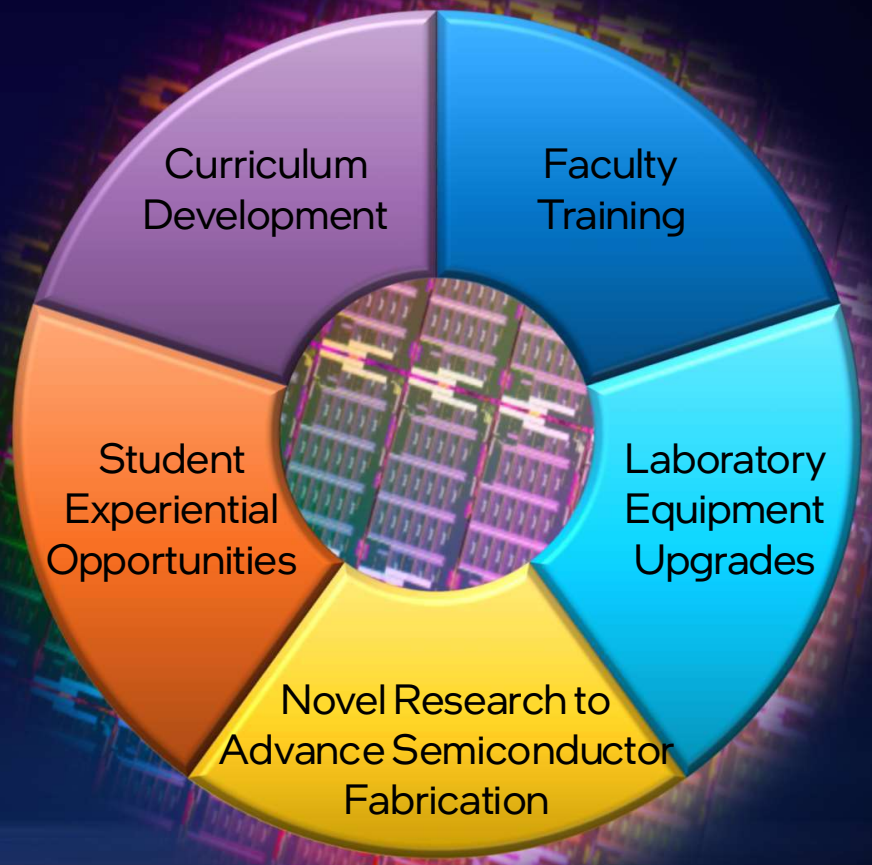
ohio let's build!

Intel® Semiconductor Education & Research Program for Ohio

Intel Breaks Ground in the Silicon Heartland today!

Intel also announced the first phase of funding for its Ohio Semiconductor Education and Research Program.

During this first phase, Intel is providing $17.7 million for eight proposals from leading institutions and collaborators in Ohio to develop semiconductor-focused education and workforce programs.



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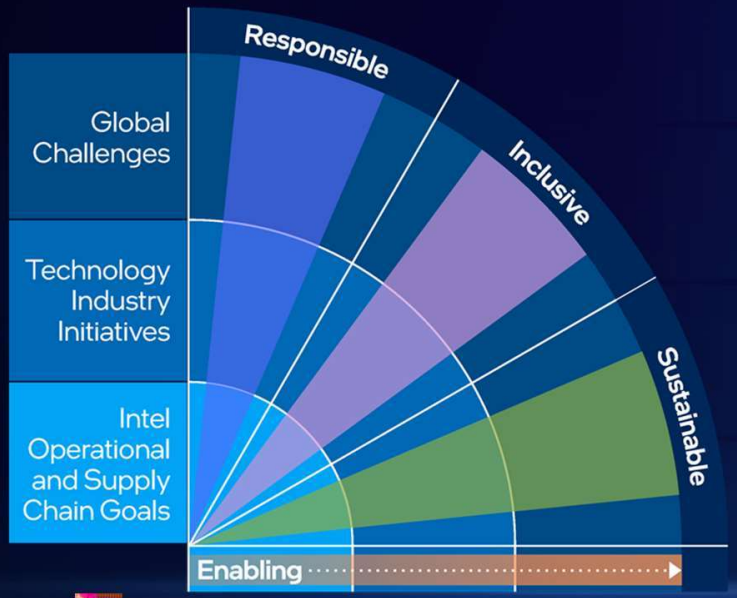
Making a Positive Impact On Society, Business, Planet

intel RISE



Responsible	Revolutionize how technology will help improve health and safety	
Inclusive	Make technology fully inclusive and expand digital readiness	
Sustainable	Achieve carbon neutral computing to address climate change	
Enabling	Accelerate the ways we enable progress through our technology and the expertise and passion of our employees	

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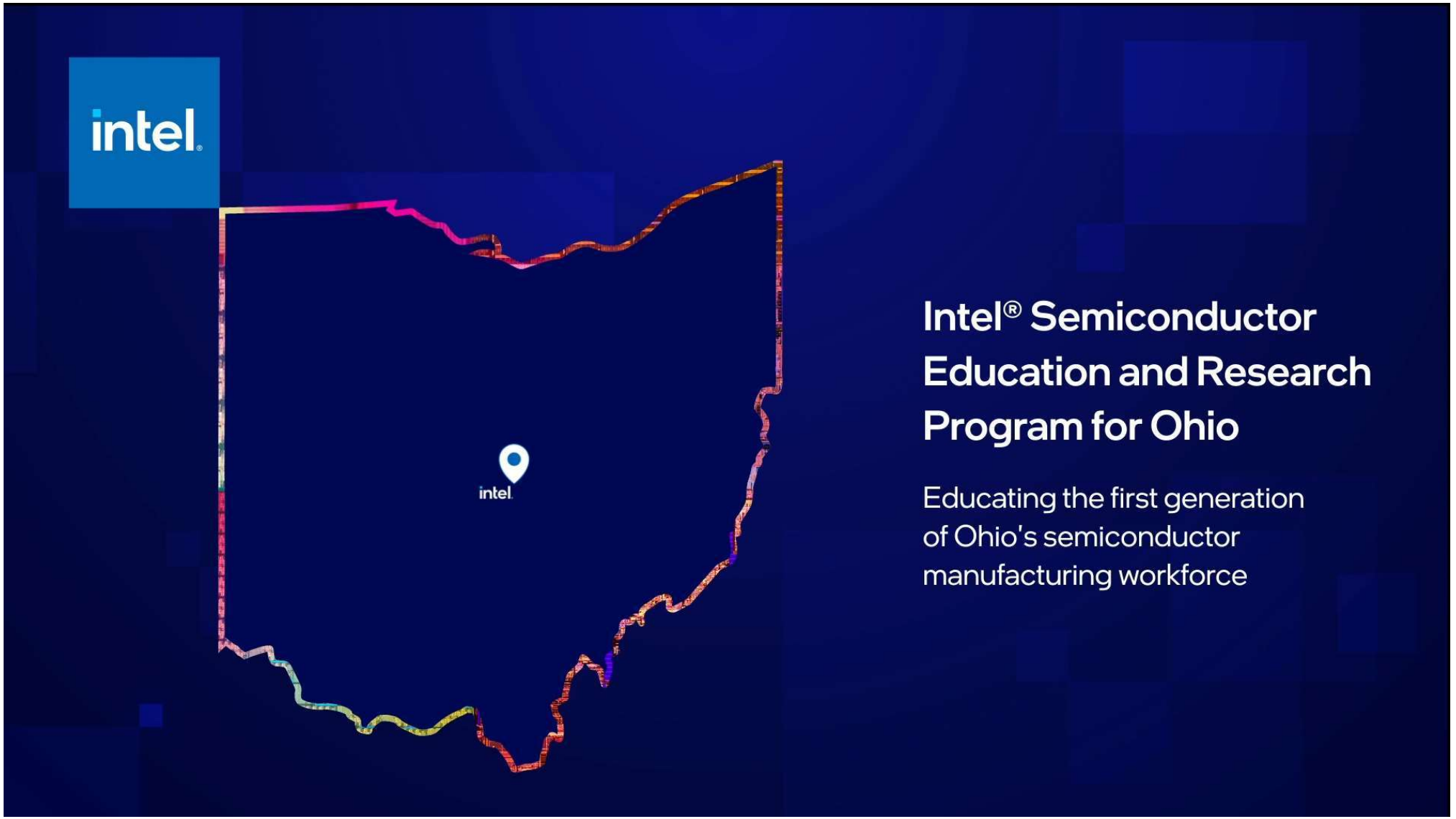
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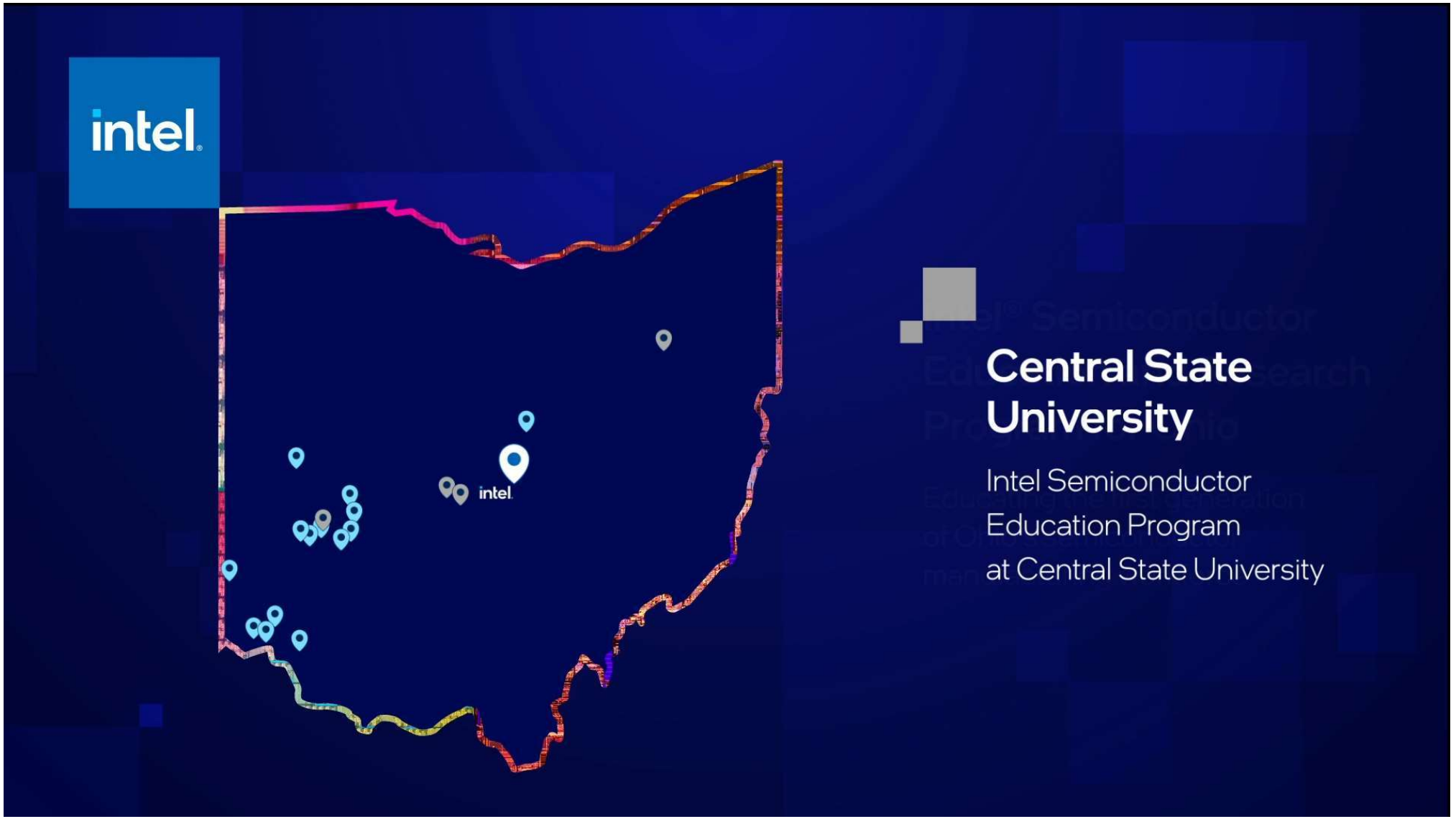
Intel® Semiconductor Education and Research Program for Ohio
Educating the first generation of Ohio's semiconductor manufacturing workforce


intel
intel
University
of Cincinnati
Ohio-Southwest Alliance
on Semiconductors
and Integrated
Scalable-Manufacturing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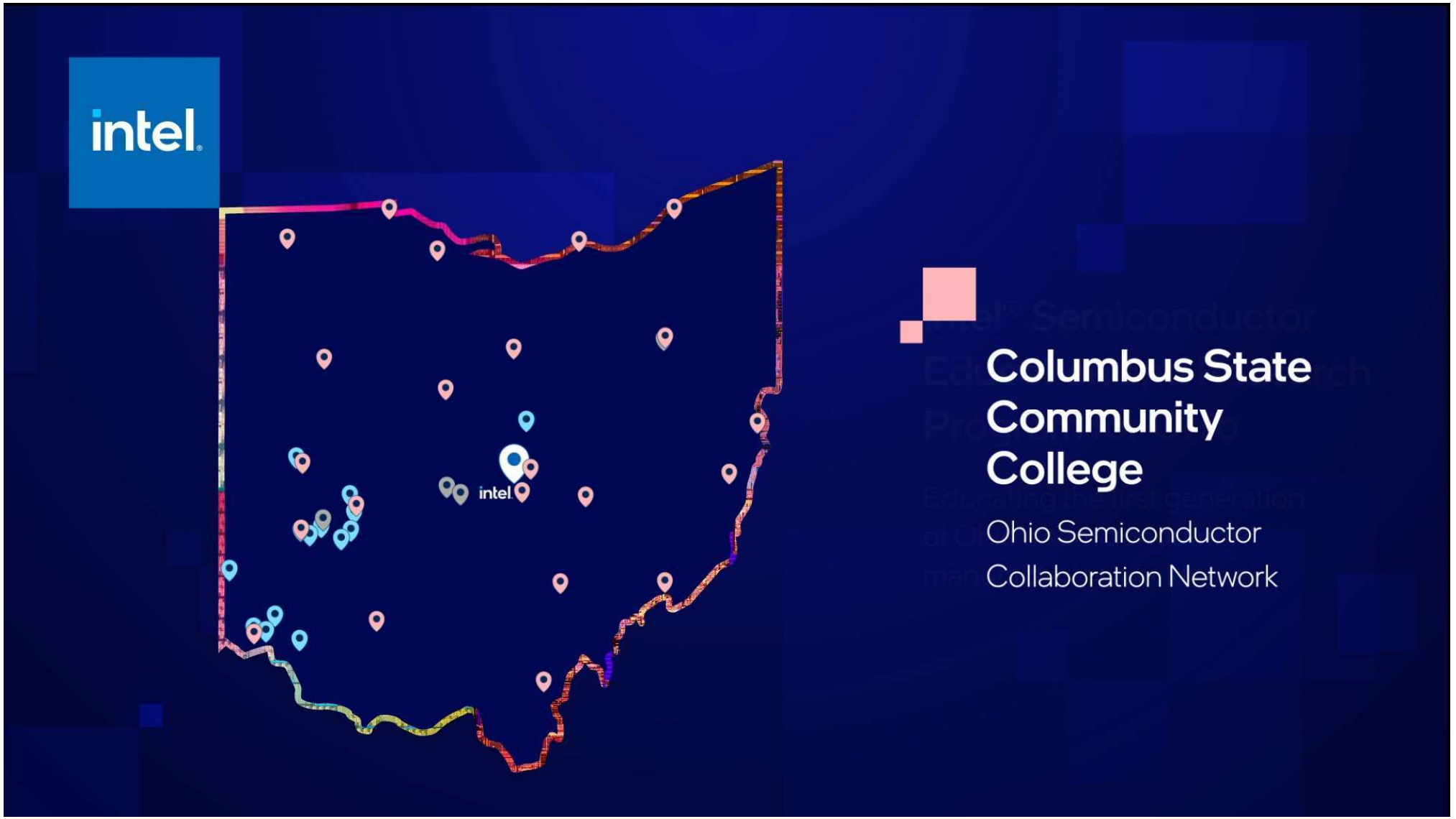
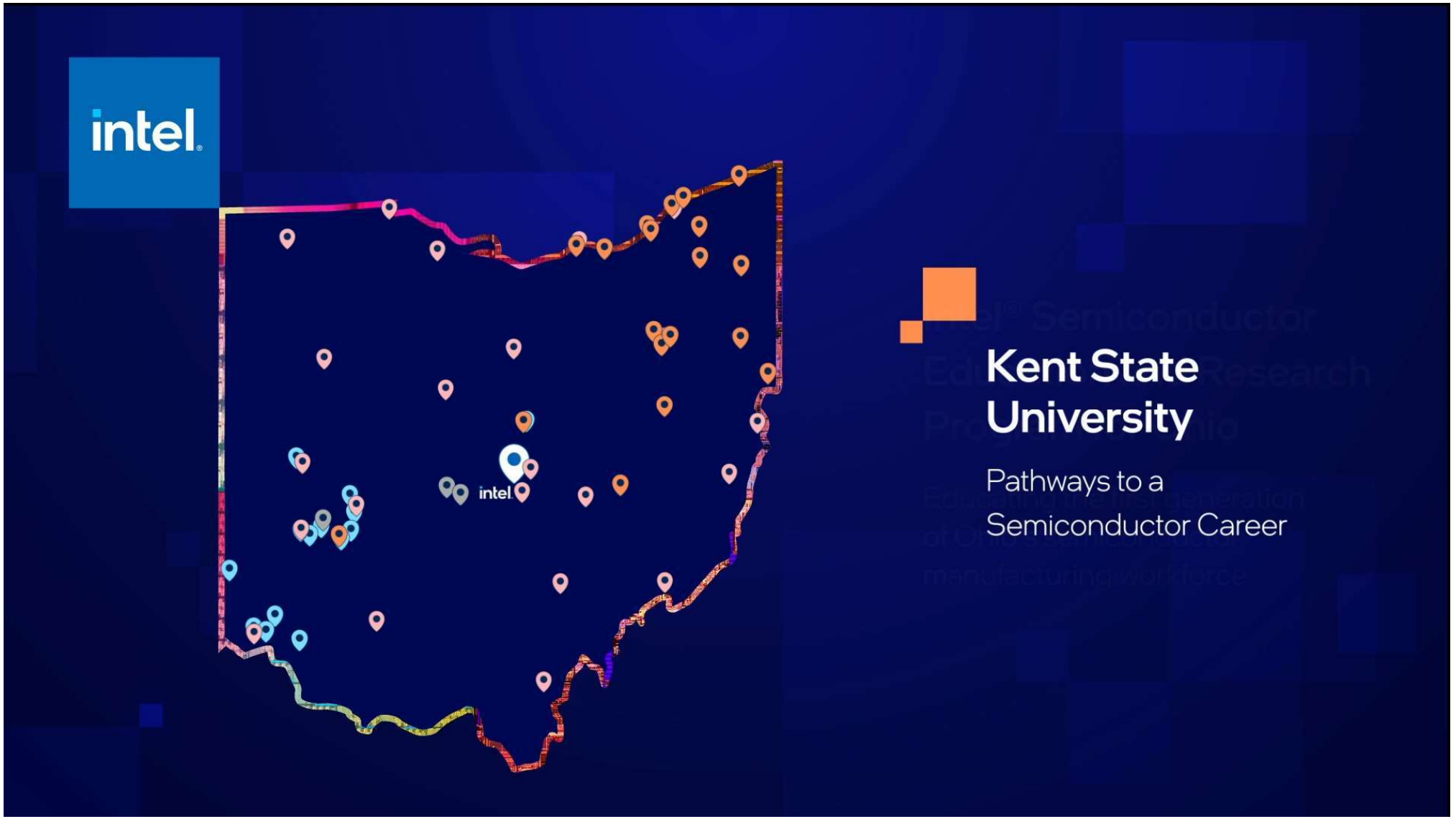
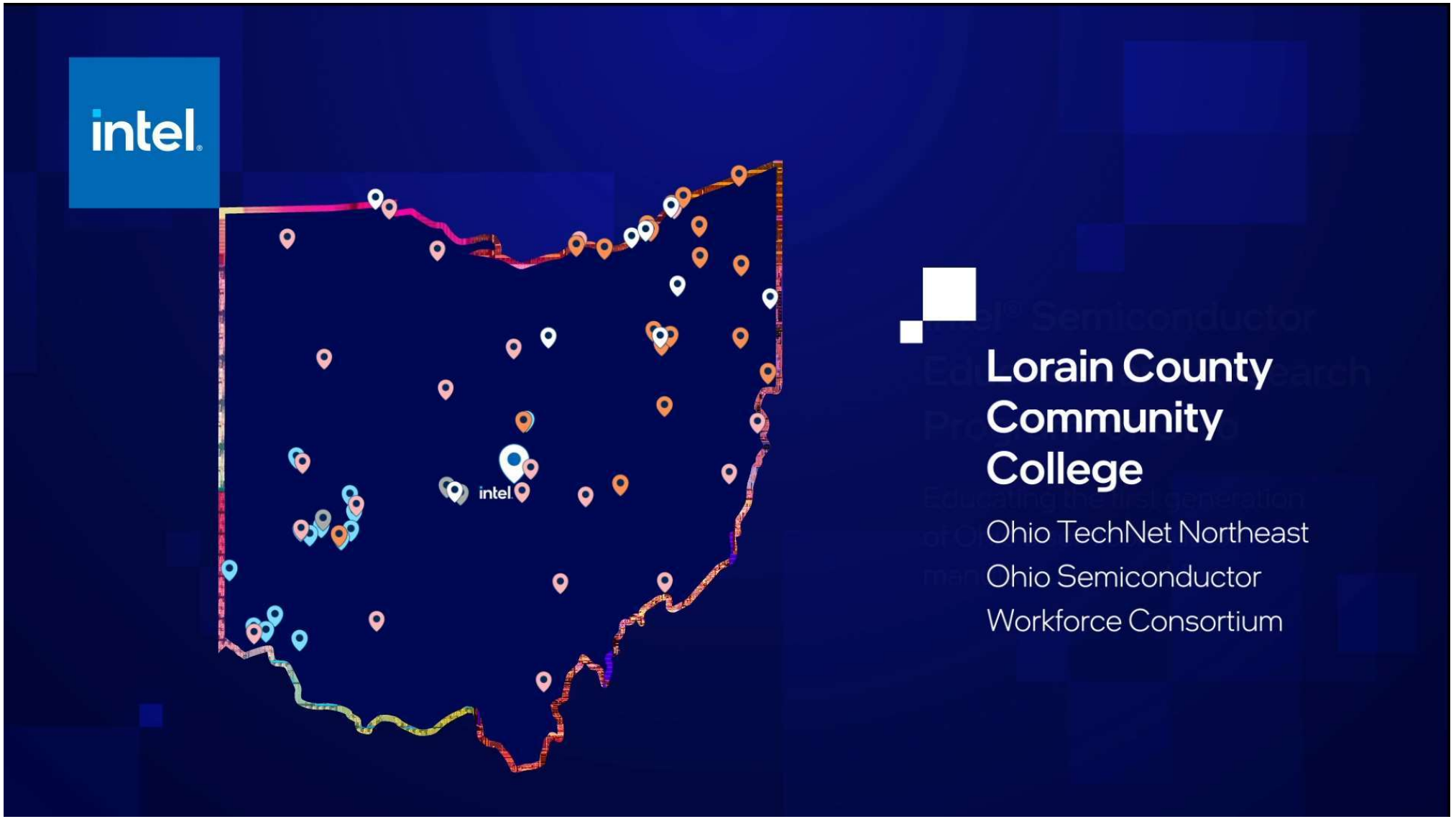
Central State University
Intel Semiconductor Education Program at Central State University


intel
Columbus State Community College
Ohio Semiconductor Collaboration Network



Kent State University

Pathways to a Semiconductor Career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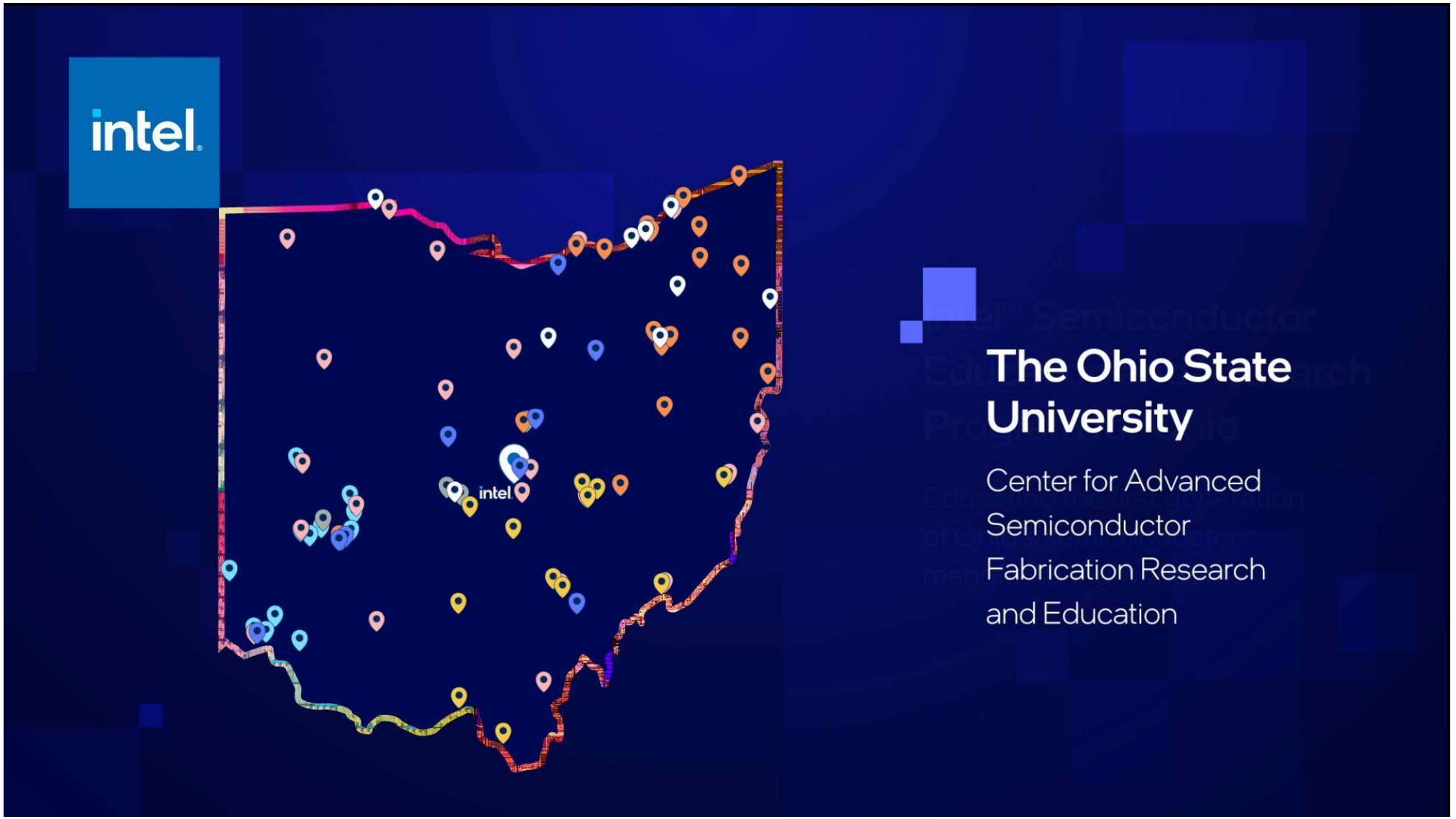
Lorain County Community College
Ohio TechNet Northeast
Ohio Semiconductor Workforce Consortium

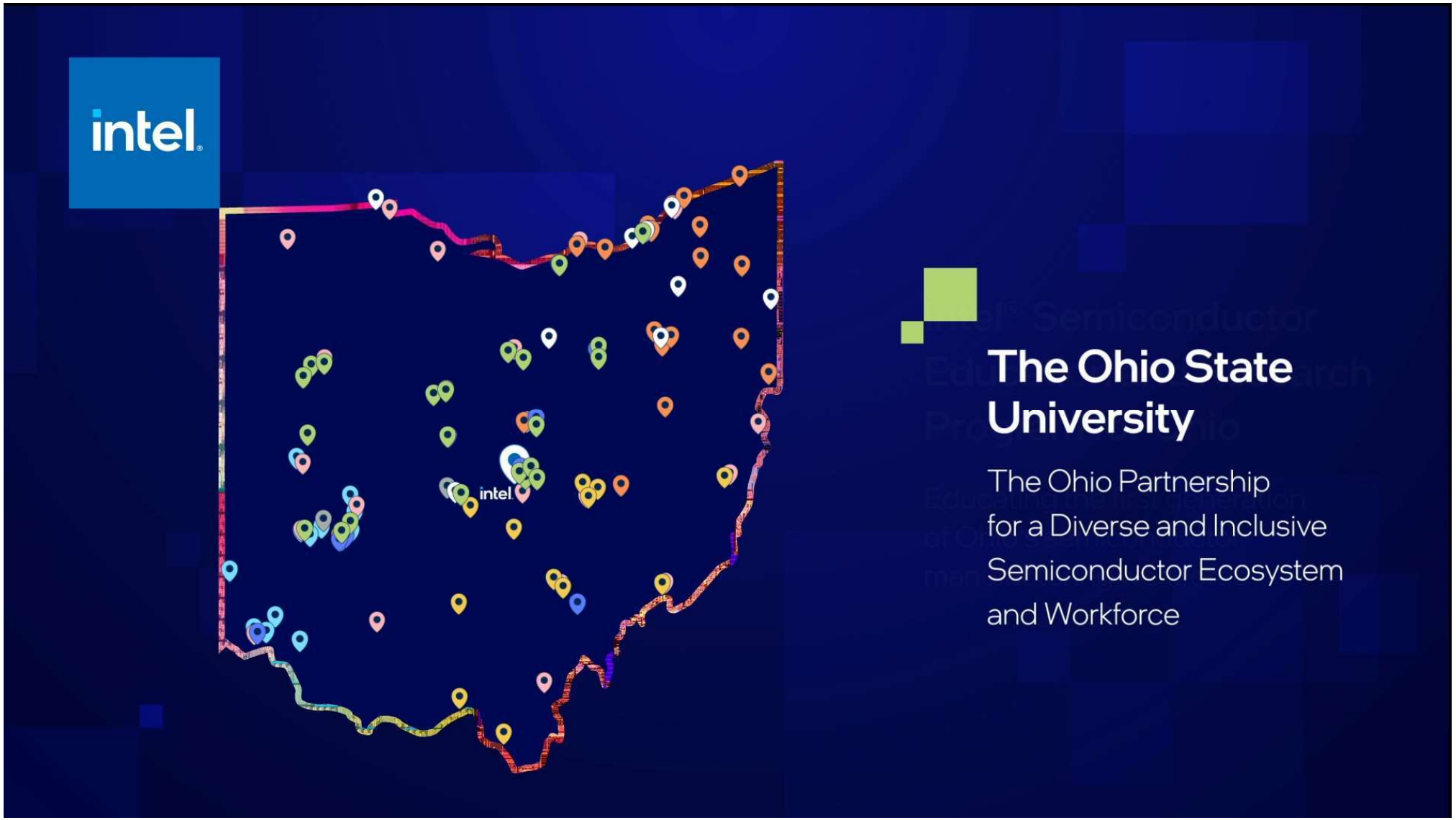
Ohio University

Appalachian Semiconductor Education and Technical Ecosystem



The Ohio State University

Center for Advanced Semiconductor Fabrication Research and Education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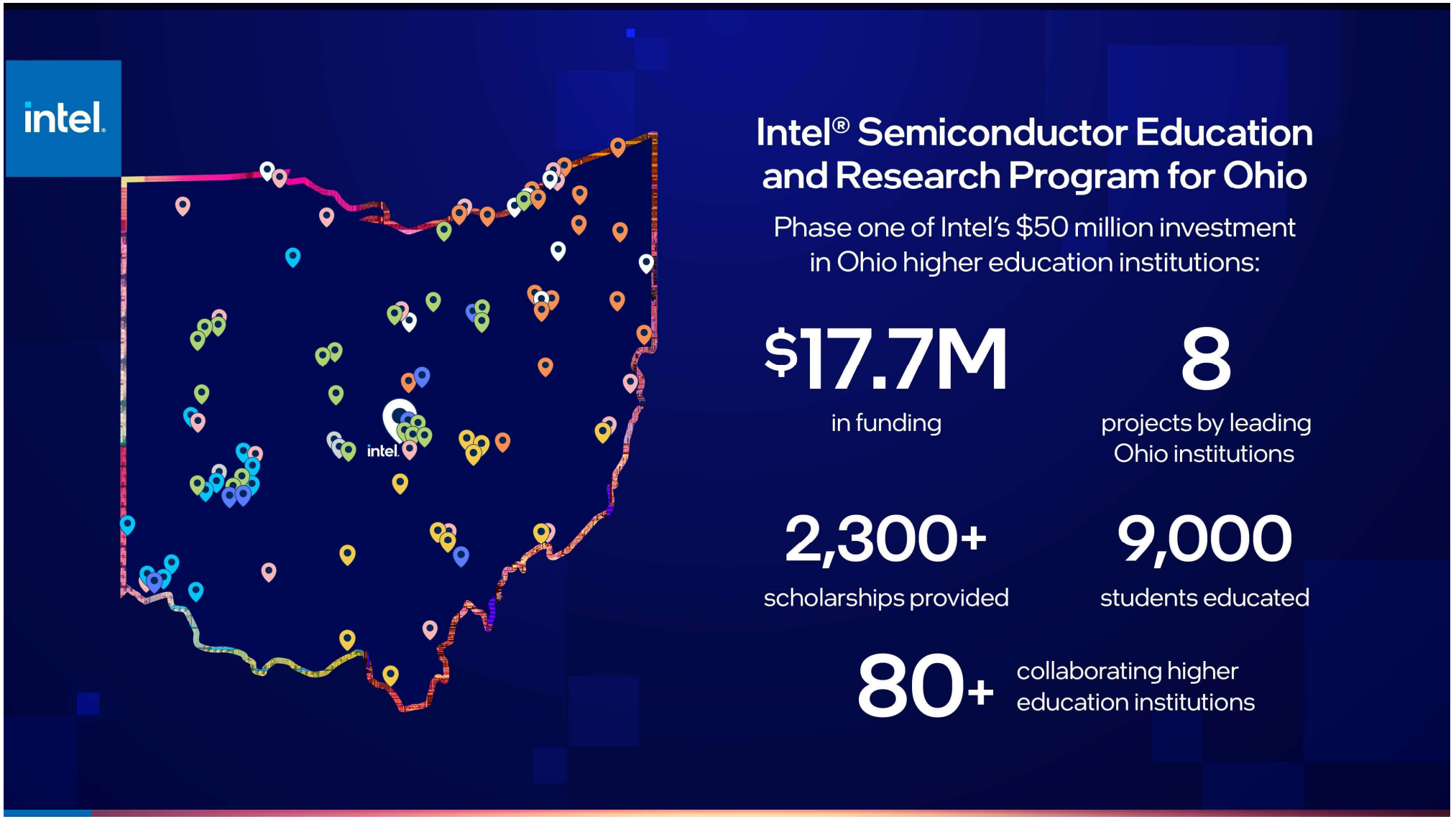
The Ohio State University
The Ohio Partnership for a Diverse and Inclusive Semiconductor Ecosystem and Workforce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Intel® Semiconductor Education and Research Program for Ohio
Phase one of Intel's $50 million investment in Ohio higher education institutions:
$17.7M
in funding
8
projects by leading Ohio institutions
2,300+
scholarships provided
9,000
students educated
80+
collaborating higher education institutions

Intel Invests $100 Million in Ohio and National Semiconductor Education and Research

$50 Million

$50 Million + **$50** Million Match

NSF

intel

Intel Invests $100 Million in Ohio and National Semiconductor Education and Research

$50 Million + $50 Million Match

NSF

On Sep 8th, NSF announced $10 million partnership with Intel Corporation to train and build a skilled semiconductor manufacturing workforce → Dear Colleague Letter (DCL)

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Q&A
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Day in a Life of an Intel Manufacturing Technician

https://youtu.be/juKOgtpD7P4

Job Opportunities

Raising the bar and evolving our corporate responsibility strategy to increase the scale of our work with others to create a more responsible, inclusive, and sustainable world, enabled through technology and our collective actions. Intel has various internships and full-time job opportunities, focused on accelerating progress against the world's critical challenges, by employing great talent with skills in:

Research: Artificial-Intelligence-Research; Security Research

Manufacturing & Facilities: Technician, Process/Yield Eng, Eng Managers, Corporate Services, Supply Chain, Quality & Reliability, Facilities, etc.

Software: Applications, Firmware and BIOS, Network Eng, Operating System Eng, Systems Eng, Test, Validation & Verification Eng, Linux Kernel Eng, RF Design, Software Development Eng, Graphics, Cloud, etc.

Hardware: Logic Design, Analog, Physical Design, FPGA, Quality & Reliability, Hardware Research & Development, Platform Eng, System Validation, etc.

System on a Chip: Design Eng, RTL Integration, Physical Design, Verification Eng, Digital Design, Memory Design & Development (NVM), Structural Design, etc.

Silicon Photonics: RX Chip Design & Integration, Circuit Design, Optical & Laser Eng

Information Technology: Security, Data Analyst, Support Technician, Network Specialist, etc.

Artificial Intelligence: Data Science, Artificial Intelligence Software & Hardware, Machine Learning, Deep Learning, Business & Research Development, Data Analytics, etc.

Sales & Marketing: Marketing, Customer, Partner, Field & Technical Sales, etc.

Business: Organization Design, Talent, Compensation & Benefits, Human Resource Specialist, Project/Program Manager, Operations, Finance Analyst, Accounting, Business, etc.

Intel Job Listing (for internships or full-time) Intel Scholars Program

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Intel technologies may require enabled hardware, software or service activation.

No product or component can be absolutely secure.

Your costs and results may vary.

Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.

All product and service plans, roadmaps, and performance figures are subject to change without notice. Process performance parity and leadership expectations are based on performance-per-watt projections. Future node performance and other metrics, including power and density, are projections and are inherently uncertain. Learn more at www.Intel.com/ProcessInnovation.


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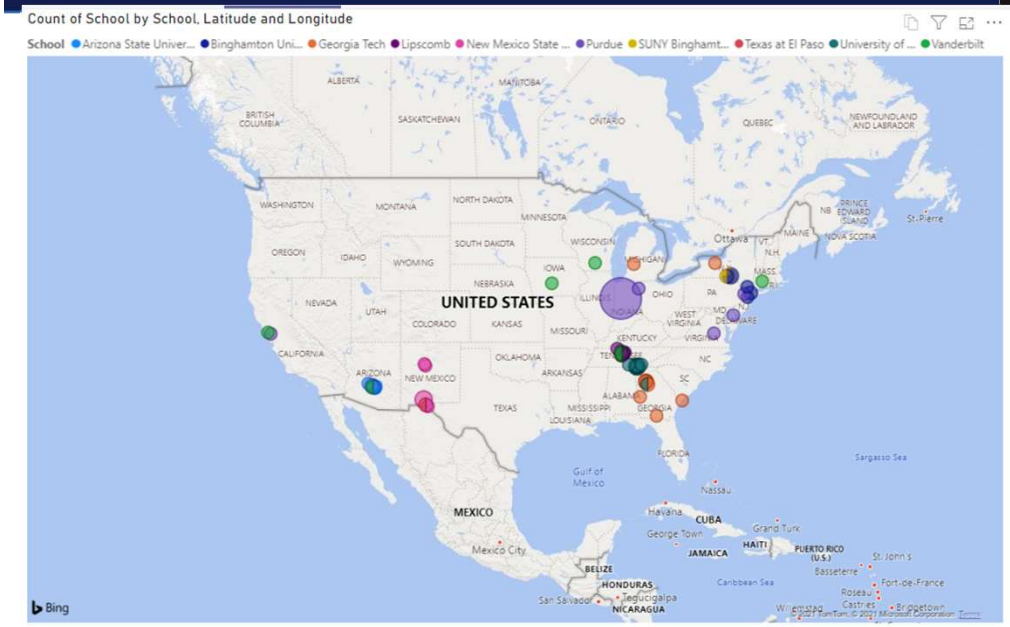
USD(R&E)

Workforce Development Overview

A ready workforce is required for the U.S. to lead rad-hard microelectronics for decades to come

Professor Peter Bermel
Purdue University
SCALE PI
pbermel@purdue.edu

SCALE is a prototype providing DOD/GOV/DIB with an asymmetric microelectronics workforce advantage



KEY

Target Institutions

Government | Federally Funded Research and Development Centers | Industry

Partners (Institution Topic Areas*)

1. Purdue University, West Lafayette, IN (RH, HIAP, SC, ESS, SC)
2. Air Force Institute of Technology, Wright-Patterson Air Force Base, OH (RH)
3. Arizona State University, Tempe, AZ (RH, HIAP, SC)
4. Brigham Young University, Provo, UT (RH)
5. Carnegie Mellon University, Pittsburgh, PA (ESS, SoC)
6. Draper Laboratory, Campridge, MA (RH)
7. Georgia Institute of Technology, Atlanta, GA (RH, HIAP, SC, ESS, SoC)
8. Indiana University, Bloomington, IN (ESS, SoC)
9. Massachusetts Institute of Technology, Boston, MA (ESS, SoC)
10. Sandia National Laboratory, Albuquerque, NM (RH)
11. Sandia National Laboratory, Livermore, CA (RH)
12. St. Louis University (RH)
13. State University of New York at Binghamton, NY (HIAP)
14. University of California, Berkeley, CA (ESS, SoC)
15. University of California, San Diego, CA (ESS)
16. University of Florida, Gainesville, FL (SC)
17. University of Michigan, Ann Arbor, MI (RH)
18. Vanderbilt University, Nashville, TN (RH)

*RH = Radiation Hardened, HIAP = Heterogeneous Integration/Advanced Packaging, SC = Supply Chain, ESS = Embedded Systems Security, SoC = System on Chip)

Technical Verticals

Radiation-hardened technology:
1. Vanderbilt
2. Air Force Institute of Technology
3. St. Louis University
4. Brigham Young University
5. Arizona State University
6. Georgia Tech
7. Purdue University
8. Indiana University
9. New Mexico State University
10. UT-Chattanooga

Heterogeneous integration and advanced packaging:
1. Purdue University
2. Georgia Tech
3. SUNY-Binghamton
4. Arizona State
5. UC-Boulder

System on Chip:
1. Ohio State University
2. Georgia Tech
3. Purdue University
4. UC-Berkeley

Supply Chain Awareness:
1. Purdue University
2. University of Florida

Embedded Systems Security:
1. Indiana University
2. IUPUI
3. Notre Dame

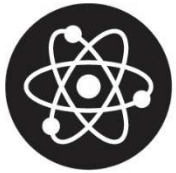
Indiana-led SCALE network includes:

- 17 universities with 287 students
- 17 federal employers
- 17 defense industry companies

For more information, see:
https://research.purdue.edu/scale/

Scope and Technical Objectives

Security. Train students and faculty in ITAR, EAR, CCL, and related regulations and to provide facilities to meet program requirements; security clearances for students.



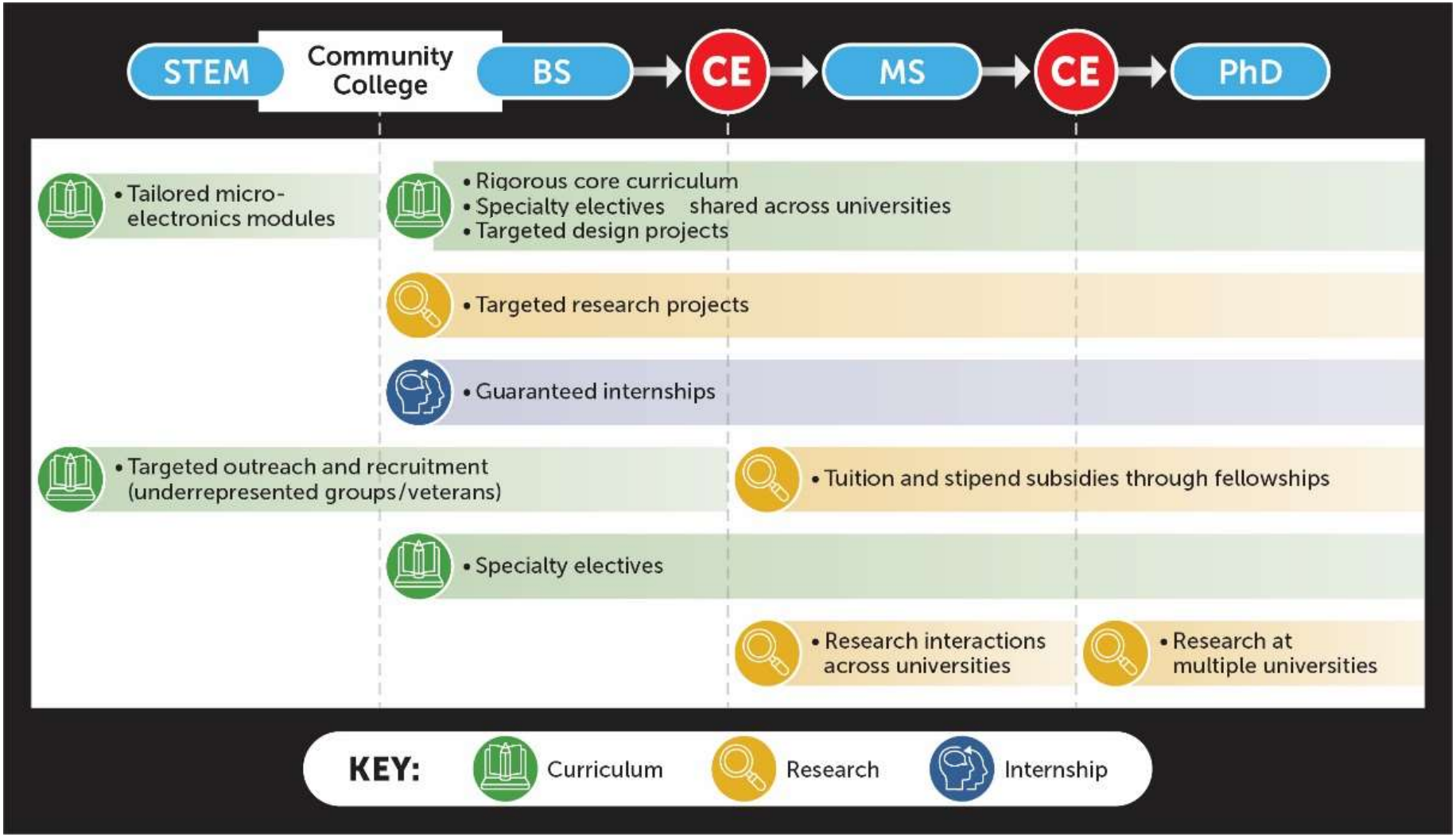
Curricular innovation. Tailored curriculum and targeted research experiences; designed based on DoD prioritized needs; collaboration between practitioners and educators.

Recruiting. Early exposure to the program including K-12 and community colleges; incentives; identity building through cohorts.

Projects, Research, and Internships. Mentored research experiences; near-peer mentoring; internships.

Metrics-driven, iterative model development. Model will be updated through an iterative, design-based method; metrics include both outcome evaluations and process assessments.

Key Program Elements for SCALE Students: K-12 through Ph.D.



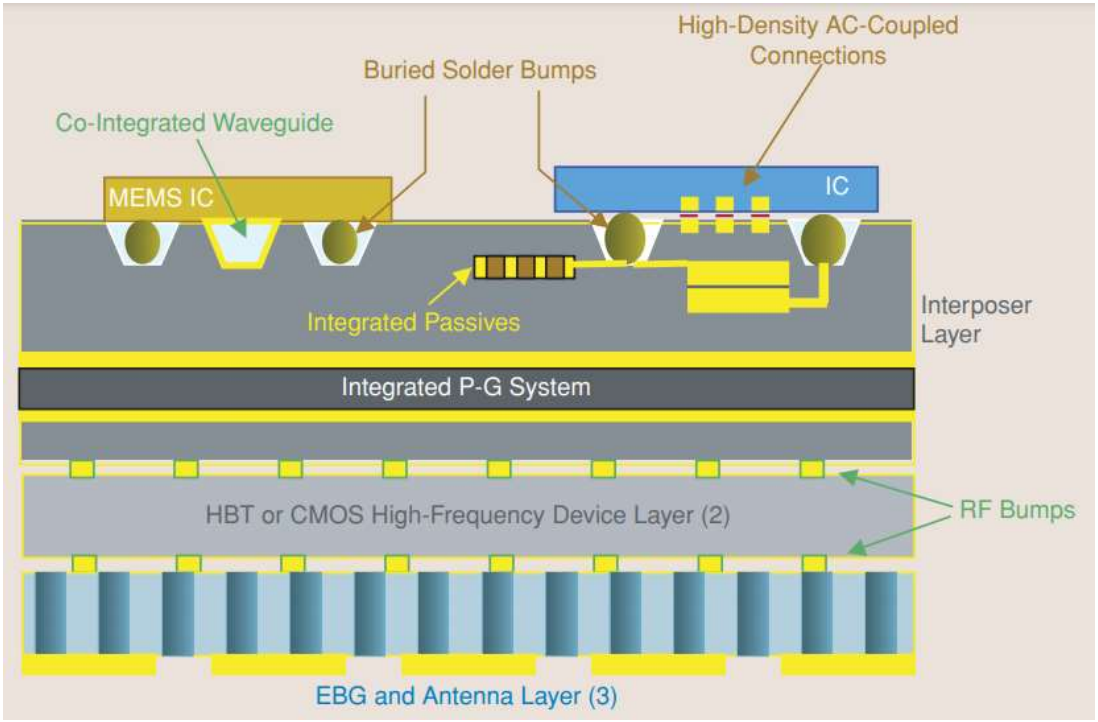
Backup Slides

Topic Areas in SCALE: Radiation-Hardened Technologies

- Radiation in natural and manmade environments can greatly affect the operation and long-term performance of microelectronics
- *Radiation hardening* is making electronic components and circuits resistant to damage or malfunction caused by high levels of ionizing radiation – either by process or
- Allows for much lighter electronics and longer mission lifetimes than would otherwise be possible
- Open questions include predicting new radiation environments, understanding potential failures for new process nodes, and rapidly testing new SOTA electronics

Topic Areas in SCALE: Heterogeneous Integration/ Advanced Packaging

- The rapid increase in chip performance associated with Moore's law has also raised interest and expectations around creating packaging devices with improved size, weight, power
- To keep sizes manageable while improving functionality, complex packaged electronics like iPhones require similar components to be compressed together horizontally and vertically, and combined with dissimilar components providing complementary functions
- Significant challenges in heterogeneous integration include designing reliable connections such as solder bumps, managing thermal cycling, and limiting damage from mechanical stress that can cause failures

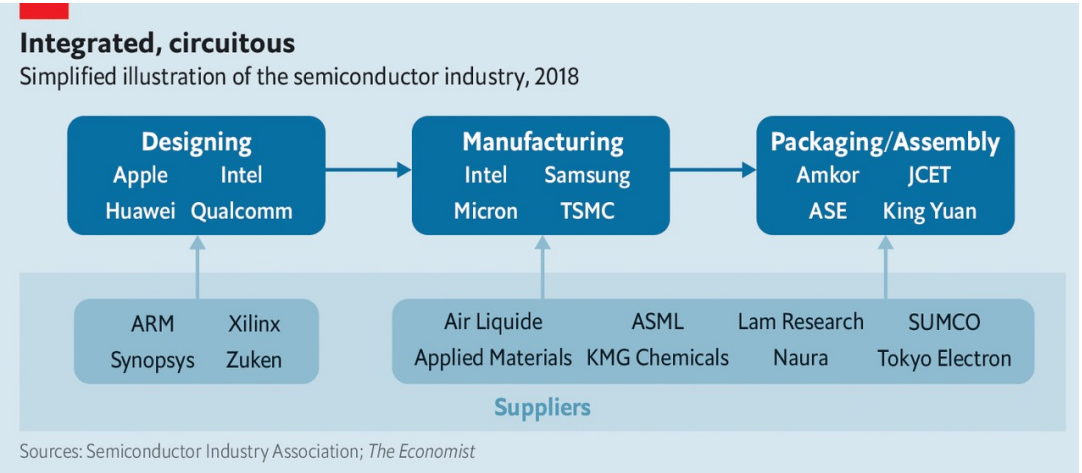


Topic Areas in SCALE: System on Chip

- Moore's law has led to an exponential increase in the number of devices that can fit onto a single chip
- This has led to a new era where most electronic systems contain chips that integrate various (hitherto discrete) components such as microprocessor, DSPs, dedicated hardware processing engines, memories, and interfaces to I/O devices and off-chip storage.
- Most electronic systems today - cell phones, iPods, set-top boxes, digital TVs, automobiles - contain at least one such System-on-chip (SoC)
- Challenges include developing a functional specifications, partitioning and mapping functions onto hardware components and software, design of a communication architecture to interconnect the components, functional/performance/power analysis and validation, and more.

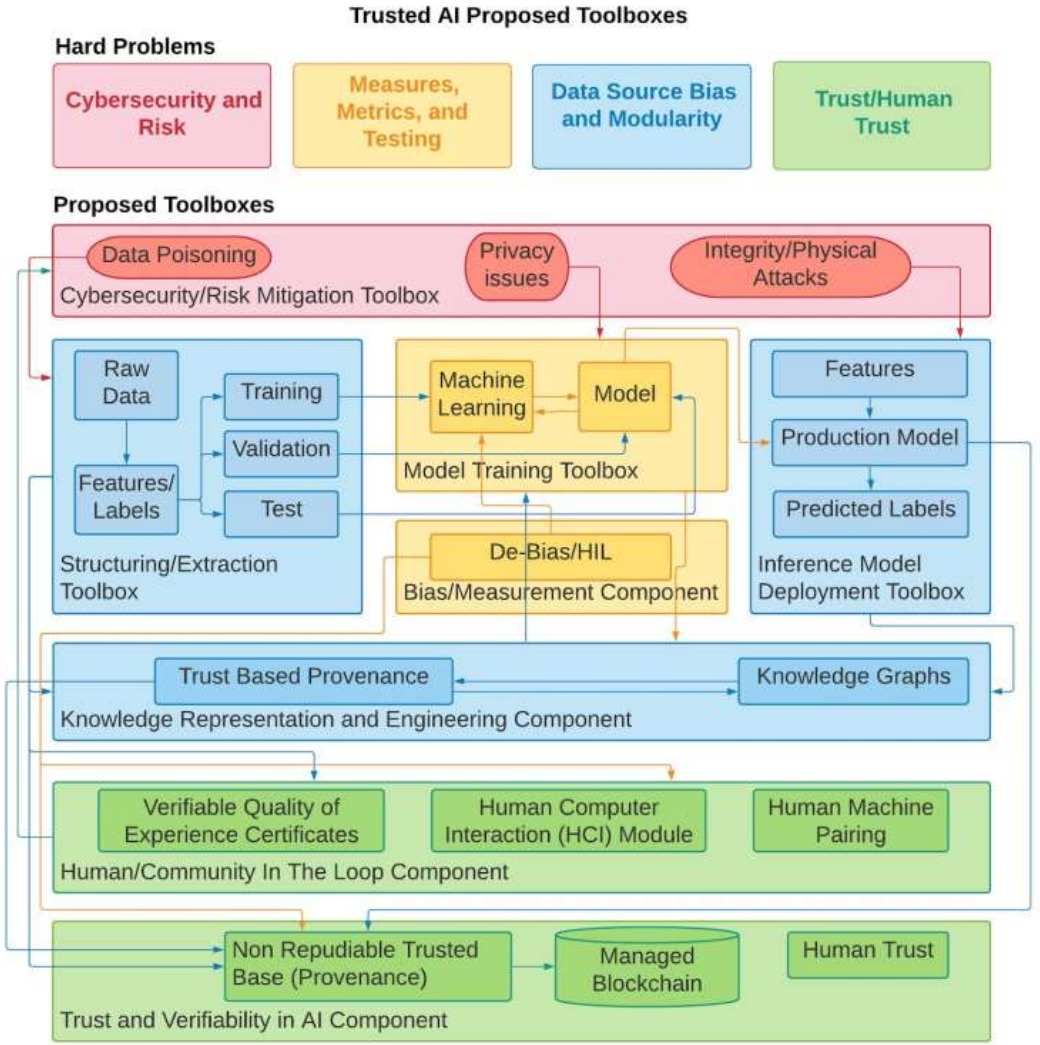
Topic Areas in SCALE: Supply Chain Awareness

- With the increasingly central role of electronic hardware in a broad range of defense applications, securing supplies of electronics is more important than ever before.
- At the same time, exponential growth and complexity in semiconductor manufacturing creates potential supply chain disruption at all levels
- Challenges include understanding potential risks of IP security, measuring and detecting potential tampering with manufacturing and packaging, as well as improving supply chain resilience



Topic Areas in SCALE: Artificial Intelligence

- Artificial intelligence (AI) provides a tremendous amount of sophisticated information analysis and decisionmaking capabilities
- AI has even been characterized as a potential third offset for DOD, if it can be trusted
- Trusted AI requires addressing hard challenges such as verifiability, bias, fairness, explainability, and human interaction and feedback



SCALE Prototype Metrics

Metric	FY20	FY21	FY 22 (Aug. 2022)	Original Goal
# SCALE Students	25	104	**288**	200
# Gov't/DIB Partners	15	26	**52**	40
# University Partners	6	9	**17**	15
# Internships	40	65	145-**243**	200
# Courses	1	4	**10**	8
# Students Reached through Courses	25	2740	2740	3250

- SCALE Prototype has met original goals of contract through FY24

Additional Potential Elements

- Competitive Fellowship and Multi-University Research Projects for Graduate Students (e.g., Draper Fellows)
- Diversity initiatives (MSIs, CCs, and MEPs)
- K-12 Outreach Efforts
- Veteran-Focused Program
- Virtual training on instrumentation (e.g., probe station use, videos, special short course on fabrication)
- Student exchanges between SCALE universities

Additional Collaborations

- Increase collaboration with stakeholders: Crane, WSMR, MDA, etc.
- Use events such as Stakeholder Discovery to explore problems of mutual interest
- Capture/increase interactions with state/local government – e.g., RFI response
- Increase collaborations with institutional support for corresponding curriculum development for faculty, plus expenses for courses like ECE 557 (Hands-On Semiconductor Fabrication)
- Leverage existing/developing course materials for multiple purposes: e.g., HI/AP course, supply chain awareness

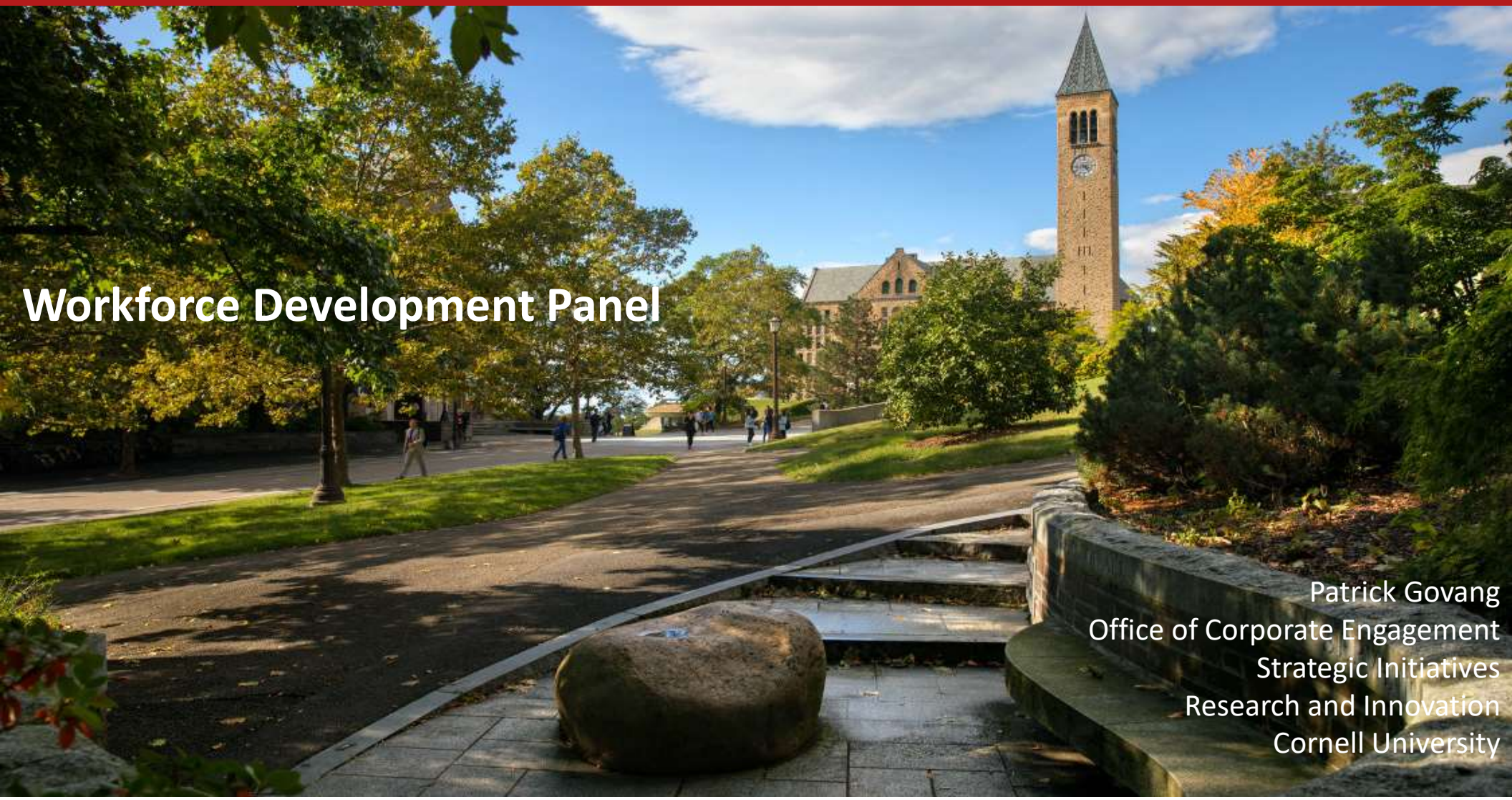
SCALE POCs

Central University POCs:

- Peter Bermel, SCALE Director – pbermel@purdue.edu
- Ed May, SCALE Managing Director – elmay@purdue.edu
- Kerrie Douglas, SRRWG Lead – douglask@purdue.edu
- Eric Holloway, SCALE Internship Coordinator – eahollow@purdue.edu

University Technical Leads

- Steve Bibyk (OSU), SOC Area Lead
- Mike Alles (Vanderbilt), RH Area Lead
- Carol Handwerker and Ganesh Subbarrayan (Purdue), HIAP Area Leads
- David Crandall (IU) and Chris Sweet (ND), ESS Area Leads



Workforce Development Panel

Patrick Govang
Office of Corporate Engagement
Strategic Initiatives
Research and Innovation
Cornell University

Workforce Development

Regional Collaboration

Full Circle View – Beyond Students

Community Colleges

National Initiatives

Seeding the Pipeline

Workforce Development

Community Colleges

Developing pilot with:

TOMPKINS CORTLAND COMMUNITY COLLEGE

Fundamentals of Micro and Nano Fabrication microcredential program

- Aligns w existing Community College degree programs
- CNF New User Orientation - Cleanroom etiquette
- Technology and Characterization at the Nanoscale (TCN) Short Course
  - Basic and advanced photolithography
  - Wet etching
  - Plasma etching (dry etching)
  - Electron beam lithography
  - Imaging (microscopy and advanced microscopy)
  - Metrology (measurement of various material properties)

Workforce Development

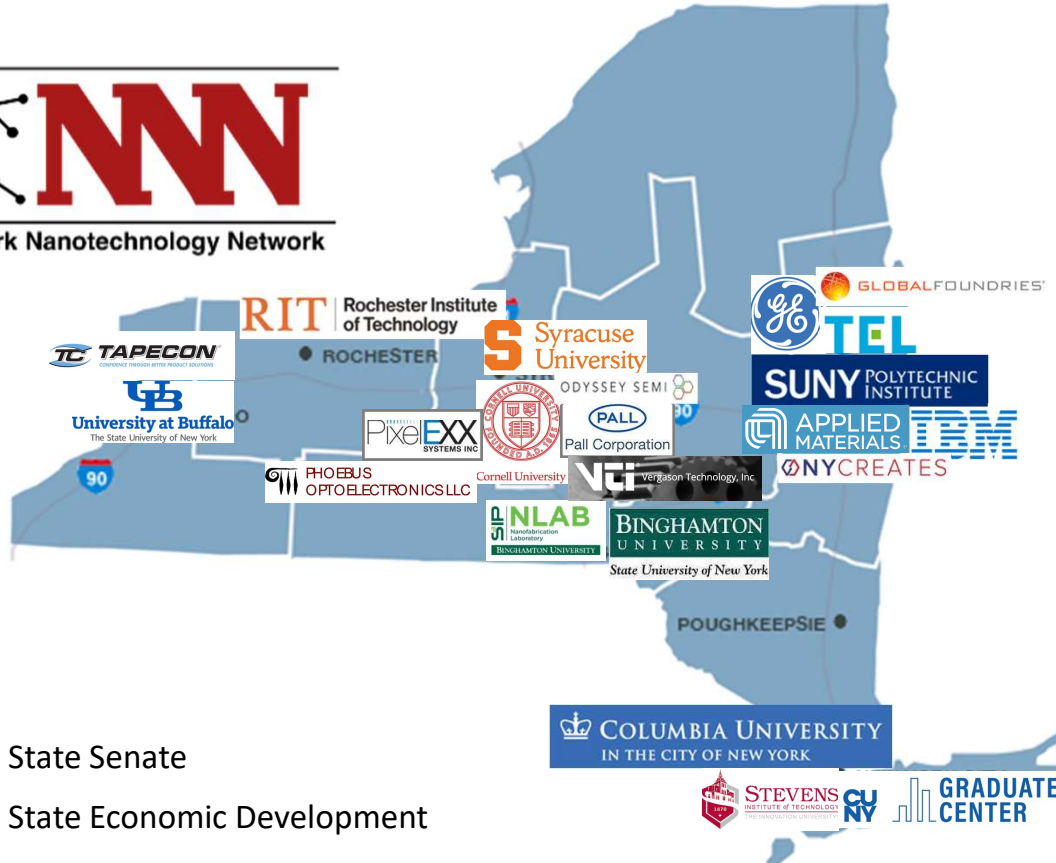
Regional Collaboration

New York Nanotechnology Network

"**Bridging the Workforce Gap**"

- Connect NYS undergraduate and graduate students with industry partners
- Showcase the NYS student talent pipeline
- Unite New York State colleges, universities and industries

Industry and Universities represented



- A total of 95 stakeholders
- 12 different NYS academic institutions
- 20 NYS companies

- NY State Senate
- NY State Economic Development
- NNCO (the National Nanotechnology Coordinating Office)

Workforce Development

National Initiatives

National Nanotechnology Coordinated Infrastructure

NSF

ASiC American Semiconductor Innovation Coalition

AMERICAN SEMICONDUCTOR ACADEMY (ASA) INITIATIVE & SEMI

Workforce Development

Full Circle View – "Beyond Students"

AF/SF/DOD Staff

Technology Adoption Hub Partners

eCornell

GRIFFISS INSTITUTE

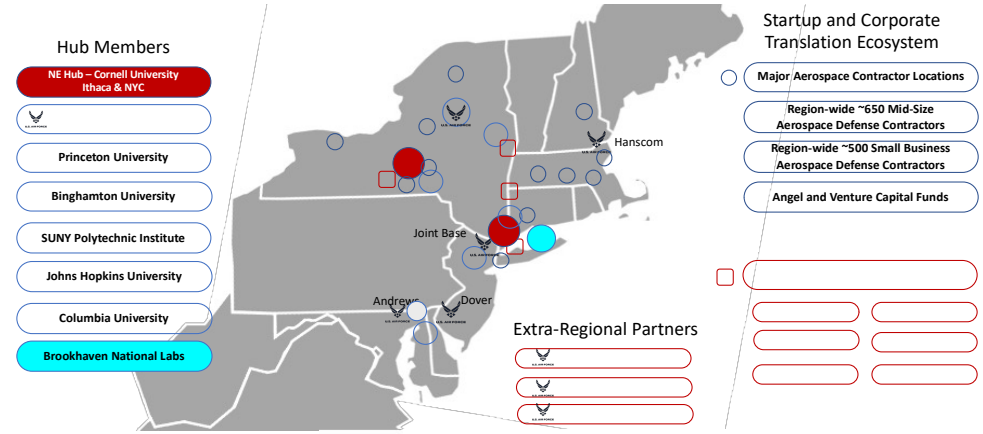
Workforce Skills Training

Graduate Student/ Post Doc E-Ship Fellows

Training for careers within AF/SF / Defense Industry

Mid - Atlantic AFRL REGIONAL HUB

U.S. AIR FORCE | USSF



Mission

Collapse the conventional path of research to products and applications; accelerate translation of ideas to intellectual property to commercialization.

Research & Entrepreneurship

Built on three core competencies:

- Integrated distributed infrastructure for accelerated data development and exploitation
- Technology transition pipeline
- Workforce development

Workforce Development

Seeding the Pipeline

CNF Cornell NanoScale Science and Technology Facility

- CNF offers "Technology and Characterization at the Nanoscale (TCN)" - semiannual 3-day laboratory and lecture-based short course
- CNF hosts REU students during summer and runs an international REU program with our partner in Japan
- Exchange program with Morgan State University, HBCU that graduates more African American electrical engineers than any other school
- Part of Quantum Leap AccelNet – a network of networks focused on Quantum Information Science
- **Outreach**: includes 4-H, Nanooze (Science news magazine distributed free to K-12 schools and edited by Cornell faculty), College /community events, first Lego, Girl Scout engineering day, NanoMeter Newsletters, Visits/tours for K-12 schools
- CNF co-located with ECE/MSE undergrad "nanomachine shop" teaching facility – **ECE 4360 - Nanofabrication and Characterization of Electronics**
- **Grad student "CNF Fellows"** – help to develop new nanofabrication processes

Microelectronics/Semiconductor Research Community Workshop

Contact:
Patrick Govang
Office of Corporate Engagement
pjg26@cornell.edu
(607) 254-2330